Schematics For 12C_RK3588S

12C_RK3588S_SCH

Main Functions Introduction

1) Charger: 1Cell Battery_QC or 2Cell Battery_QC or 3Cell Battery_QC
2) PMIC: 1 x RK806-1+DiscretePower
3) RAM: 2 x 32bits LPDDR4/4x or 2 x 32bits LPDDR5
4) ROM: eMMC5.1(Default) or SPI Falsh
5) Support: 1 x Micro SD Card3.0
6) Support: 1 x Type-C 3.0(with DP function) +1 x USB2.0 HOST + 1 x USB3.0 HOST
7) Support: 2 x 4Lanes MIPI D/CPHY RX Camera
8) Support: 2 x 2Lanes MIPI DPHY RX Camera
9) Support: 1 x HDMI2.1 TX or 1 x eDP1.3 TX
10) Support: 2 x 4Lanes MIPI D/CPHY TX
11) Support: a/b/g/n/ac/ax 2T2R WIFI(PCIE) + BT5.0
Or: a/b/g/n/ac 2T2R WIFI(SDIO) + BT5.0
12) Support: 1 x Headphone + 2 x Speaker out + 1 x Analog MIC
13) Support: 2 x PDM MIC Array
14) Support: Gyroscope+G-sensor+Ambient Light+Proximity +Hall Sensor

JWIPC Technology Co.,Ltd.		
Page Name: 00.Cover Page		
Size: A4	Project Name: 12C_RK3588S	Rev: V1.0
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Different with reference design

Note

The power suffix S0 or S3 means:

S3: Keep power On during sleeping

S0:Power off during sleeping

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Different

Description

Note

Option

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

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Page Name: 01.Index and Notes

Size	Project Name	Rev
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Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2022-01-05	Joseph.Wei	1:Revision preliminary version	
V0.1	2022-03-05	Kuang	1:EVT version	
V0.2	2022-06-15	Kuang	1:Add Q2100 for BAT enable 2:Finger printer SPI remove to VCCIO6 GPIO 3:Add R2266,C2267 RC SCH For auto boot up when plug in AC 4:VCCIN power rail MLCC change to 0603 size and con-lay with poscap 5:DMIC IO port change to PDM1_M1 6:Add SLP_S3_L GPIO for quick response S3 7.Change SGM3157YC6/TR to SGM2549DYN6G/TR For CTIA/OMTP Headset Ground Pole Switch 8.Change G sensor U9000 source to LIS2DW12	

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Page Name: 02.Revision History

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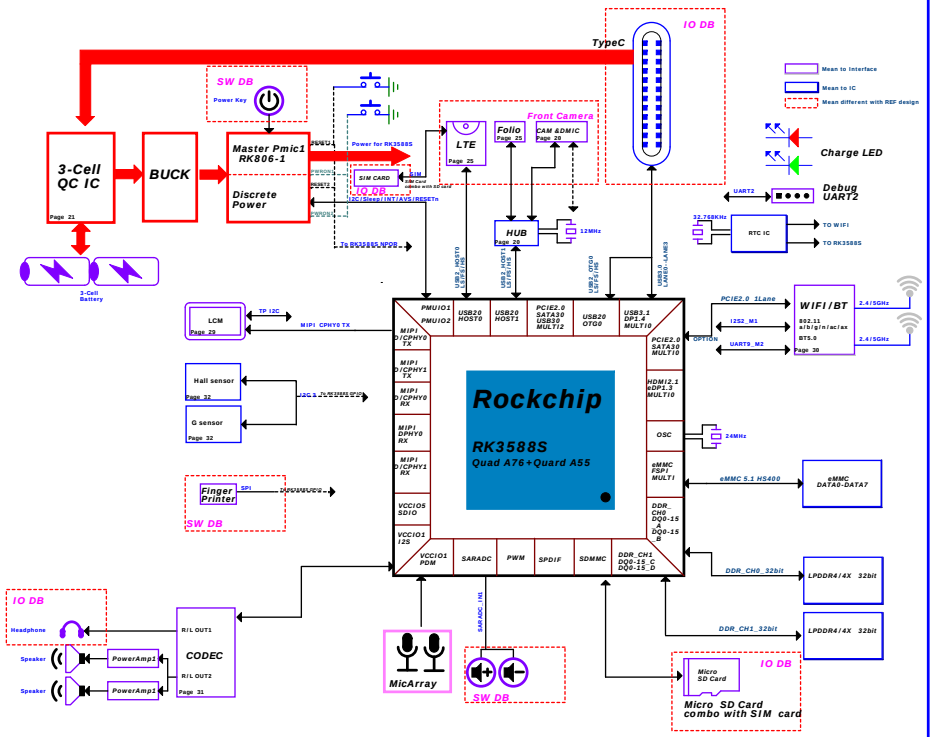
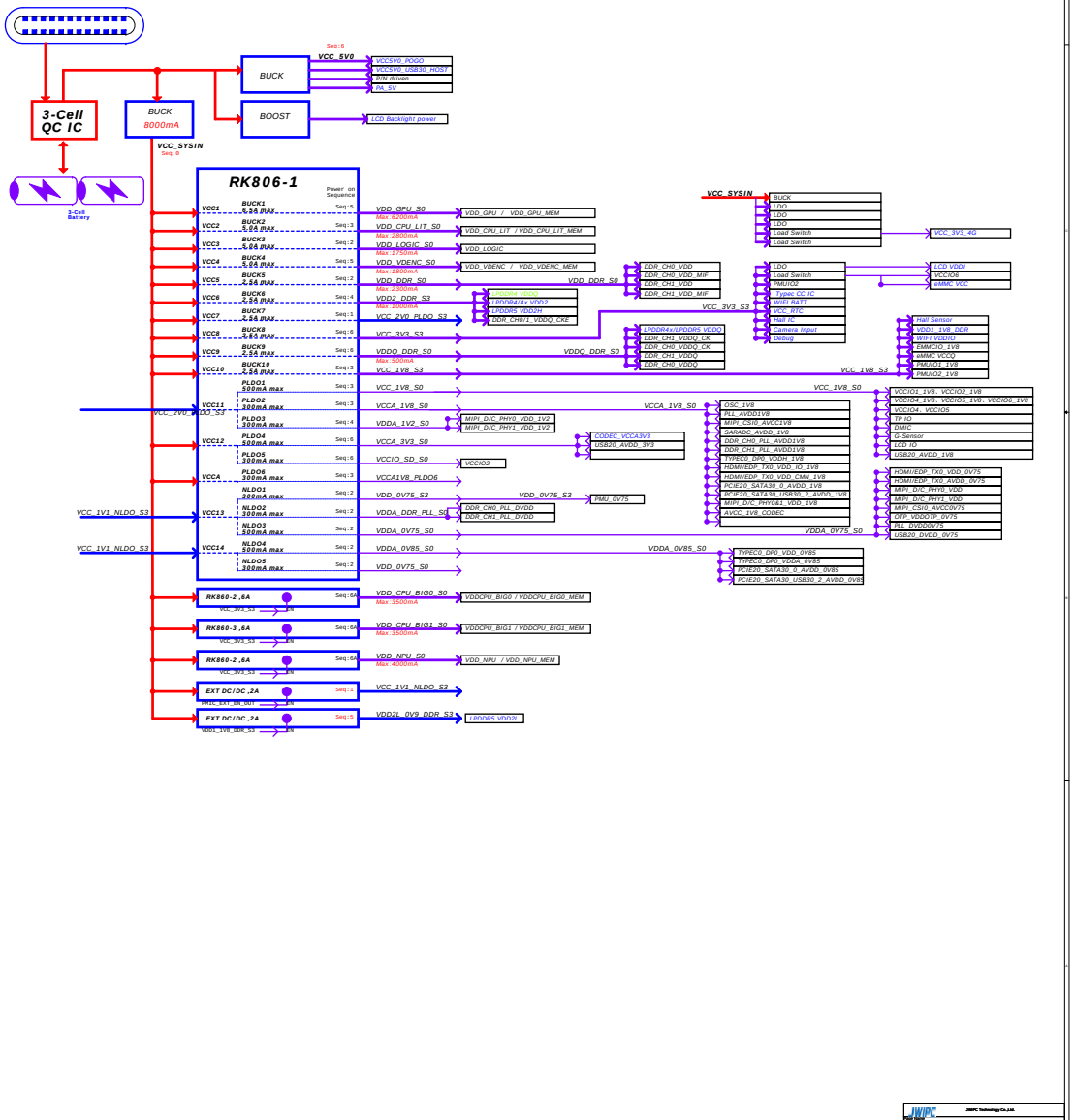
RK3588S Tablet Ref Block Diagram for 1-Cell Charger

Power tree for 1-Cell Charger

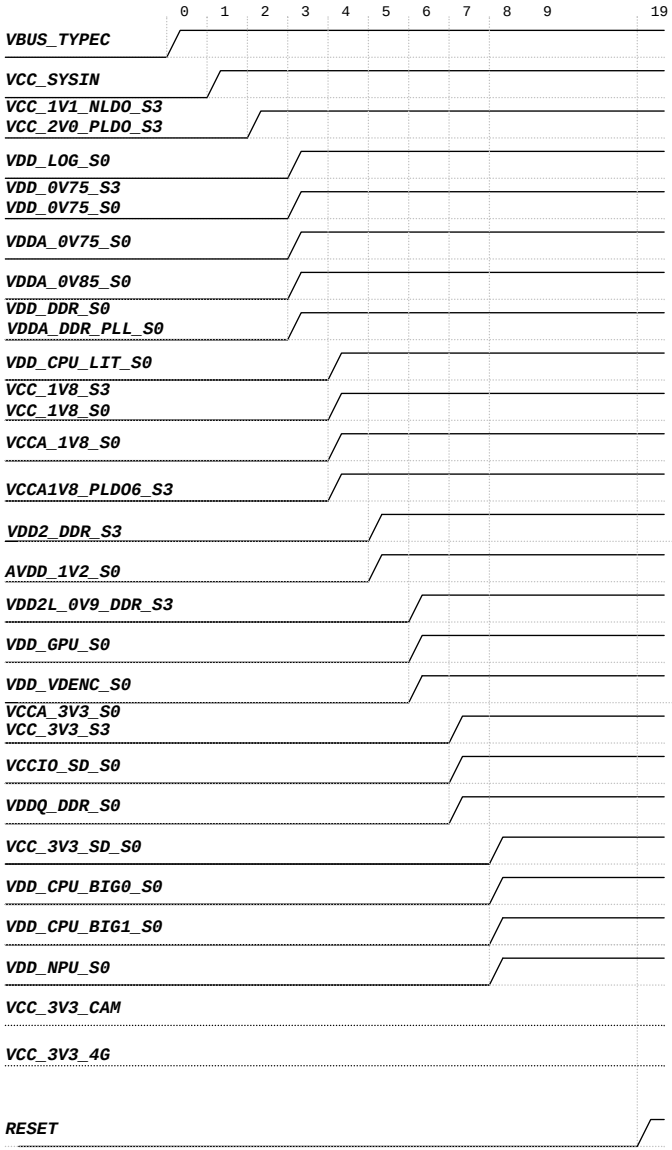
12C_RK3588S Tablet Block Diagram for 3-Cell Charger



Power tree for 3-Cell Charger



Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC_SYSIN	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO_S3	RK806-1_PLDO1	0.5A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	VDDA_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	VDD_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5	0.9V	ON	ON	TBD	TBD
VCC_SYSIN	EXT BUCK	2.5A	VCC_3V3_SD_S0	Slot:6A	3.3V	ON	OFF	TBD	TBD
VCC_SYSIN	EXT_BUCK or LDO	2A	VCC_1V2_CAM_S0	OFF	1.2V	OFF	OFF	TBD	TBD
VCC_SYSIN	LDO	0.5A	VCC_1V8_CAM_S0	OFF	1.8V	OFF	OFF	TBD	TBD
VCC_SYSIN	LDO	0.5A	VCC_2V8_CAM_S0	OFF	2.8V	OFF	OFF	TBD	TBD

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO1	Pin N36 N37	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin V37 Y37 Pin V35 V36	1.8V or 3.3V	PMUIO2_1V8 PMUIO2	VCC_1V8_S3 VCC_3V3_S3	1.8V 3.3V
EMMCIO	Pin AC35 Pin AC36	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
VCCIO1	Pin H31	1.8V Only	VCCIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AK11 Pin AK10	1.8V or 3.3V	VCCIO2_1V8 VCCIO2	VCC_1V8_S0 VCC_IO_SD	1.8V 1.8V/3.3V
VCCIO4	Pin G27 G28 Pin G31	1.8V or 3.3V	VCCIO4_1V8 VCCIO4	VCC_1V8_S0 VCC_3V3_S0	1.8V 1.8V
VCCIO5	Pin AF35 AF36 Pin AC33 AC34	1.8V or 3.3V	VCCIO5_1V8 VCCIO5	VCC_1V8_S0 VCC_1V8_S0	1.8V 1.8V
VCCIO6	Pin AJ34 Pin AL33 AM33	1.8V or 3.3V	VCCIO6_1V8 VCCIO6	VCC_1V8_S0 VCC_3V3_S0	1.8V 3.3V

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Page Name: 05.System Power Sequence

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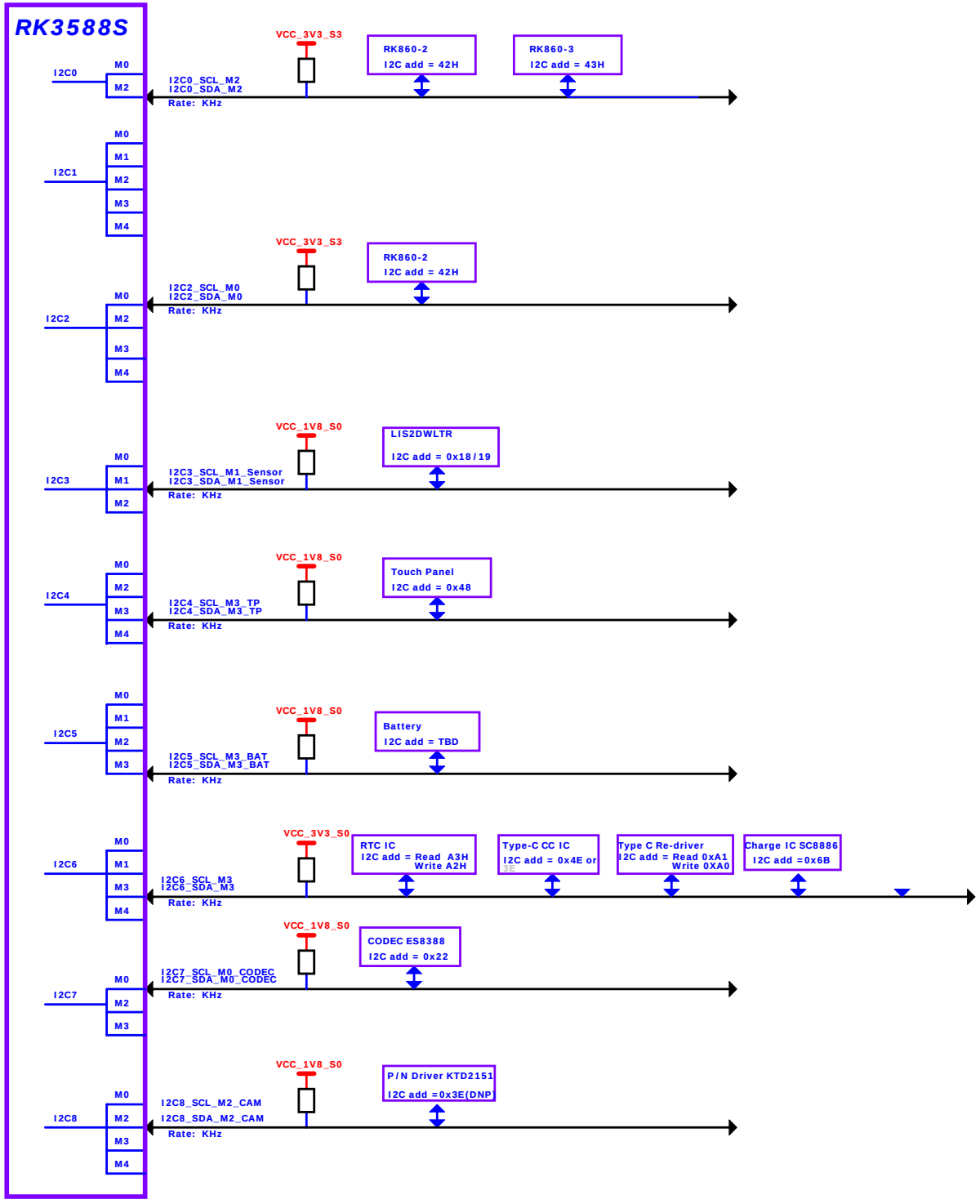
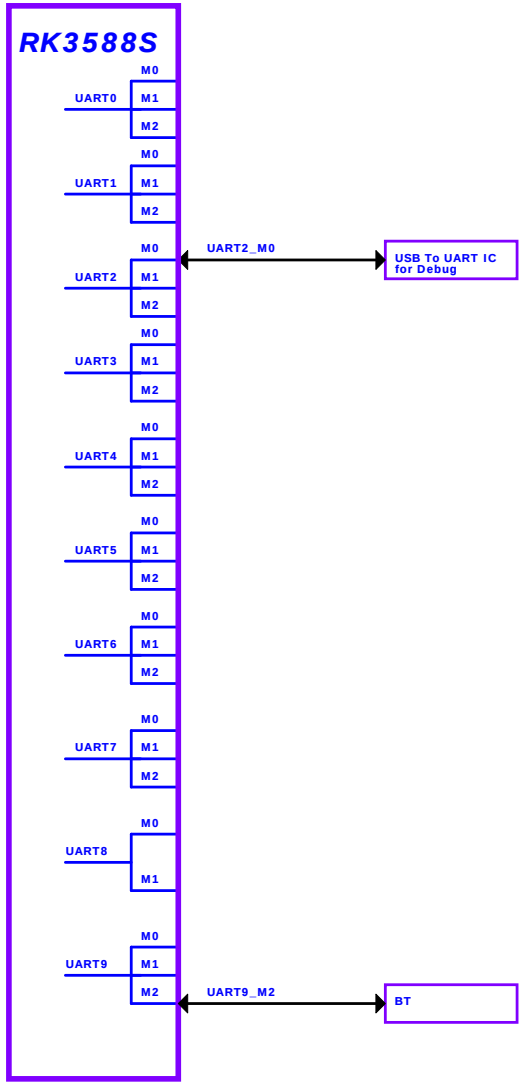
I2C MAP



UART MAP



JWIPC Technology Co.,Ltd.	
Page Name	06.Lower-Speed Bus Map
Size: A2	Project Name: I2C_RK3588S
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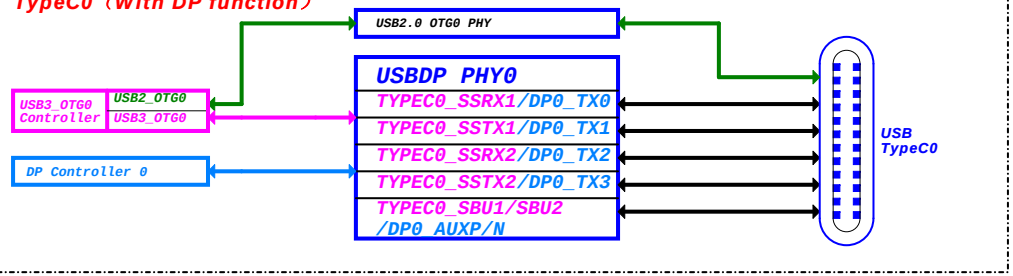
USB Controller Configure Table

Controller Name	Pin Name	Type-C Function	DPx4Lane+USB20 OTG		USB30 OTG+DPx2Lane Function		USB20 OTG+DPx2Lane Function		USB20 OTG+DPx4Lane Function	
			OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2
USB30 OTG0 Device or Host	TYPEC0_SBU1/DP0_AUXP TYPEC0_SBU2/DP0_AUXN	TYPEC0_SBU1 TYPEC0_SBU2	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN
	TYPEC0_SSRX1P/DP0_TX0P TYPEC0_SSRX1N/DP0_TX0N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX0P DP0_TX0N		DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N
	TYPEC0_SSTX1P/DP0_TX1P TYPEC0_SSTX1N/DP0_TX1N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX1P DP0_TX1N		DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N
	TYPEC0_SSRX2P/DP0_TX2P TYPEC0_SSRX2N/DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N		DP0_TX2P DP0_TX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N
	TYPEC0_SSTX2P/DP0_TX3P TYPEC0_SSTX2N/DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N		DP0_TX3P DP0_TX3N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N
USB20 OTG0 Device or Host	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM		TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM
			OPTION1 USB30 HOST		OPTION2 USB30 HOST					
USB30 OTG2 Device or Host	PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN					
	PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN					
USB20 HOST0	USB20_HOST0_DP USB20_HOST0_DM		USB20_HOST0_DP USB20_HOST0_DM							
USB20 HOST1	USB20_HOST1_DP USB20_HOST1_DM				USB20_HOST1_DP USB20_HOST1_DM					

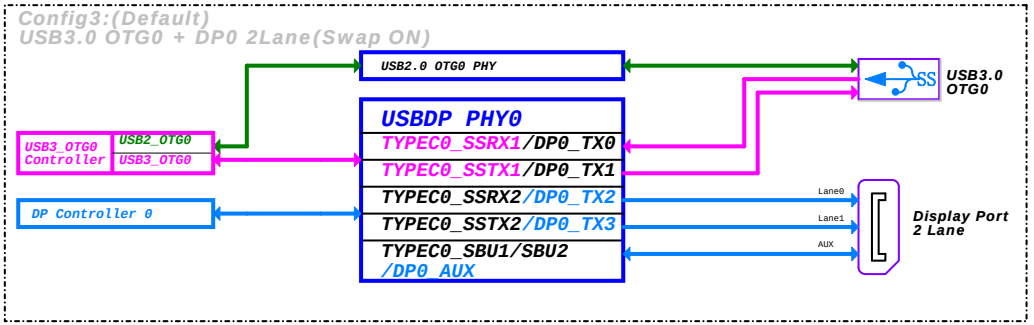
Note:
DP Lane swap enable
0:Lane0/1/2/3 TxData mapping to Lane0/1/2/3_TXDP/N
1:Lane0/1/2/3 TxData mapping to Lane2/3/0/1_TXDP/N

Note:
Red Font mean which Configure for 12C_RK3588S project

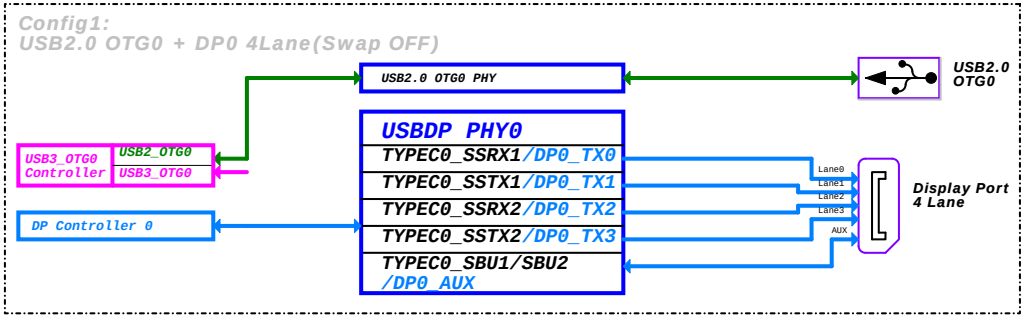
Config0:
TypeC0（With DP function）



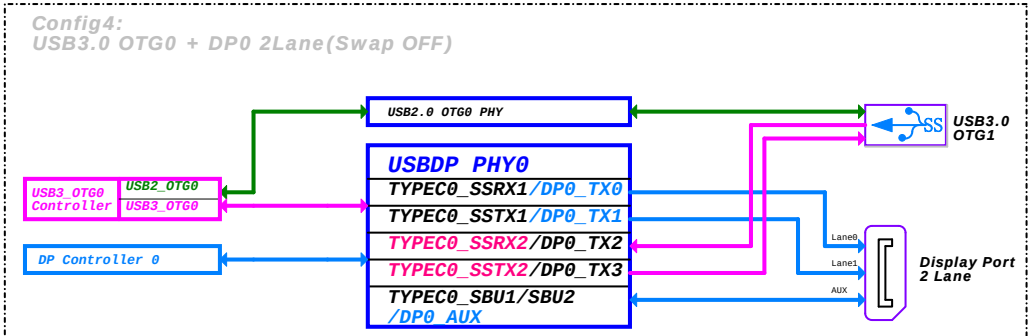
Config3:(Default)
USB3.0 OTG0 + DP0 2Lane(Swap ON)



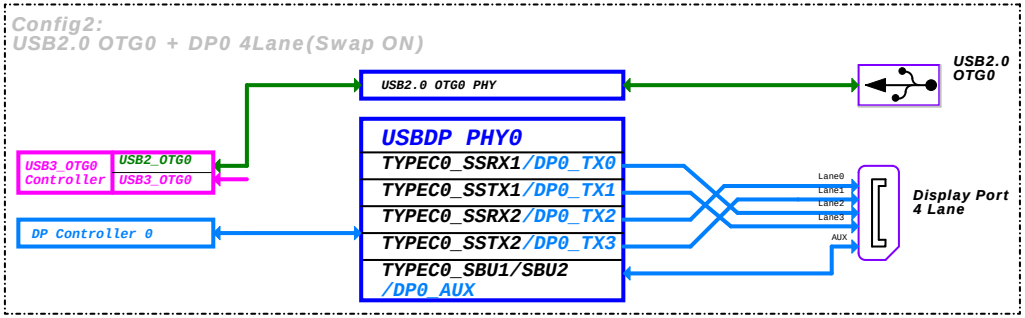
Config1:
USB2.0 OTG0 + DP0 4Lane(Swap OFF)



Config4:
USB3.0 OTG0 + DP0 2Lane(Swap OFF)



Config2:
USB2.0 OTG0 + DP0 4Lane(Swap ON)



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Page Name: 07.USB Controller Configure Tab
Size: A1 | Project Name: 12C_RK3588S | Rev: V1.0
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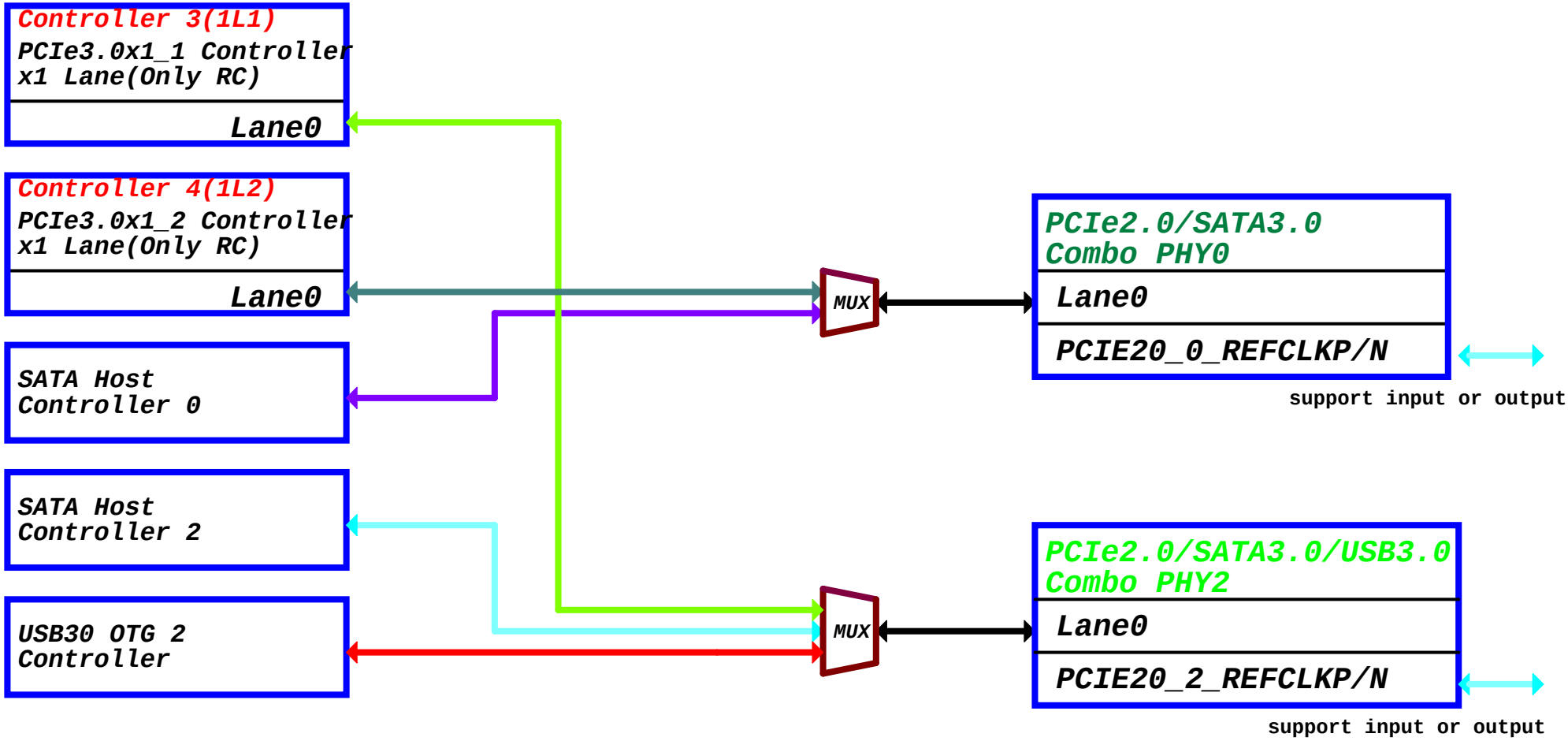
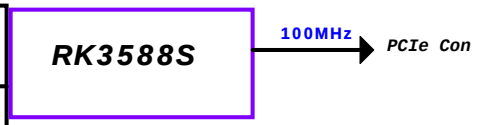
PCIe/SATA Connecter Diagram



PCIe Controller Configure Table

Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ_M* PCIE20X1_1_WAKEN_M* PCIE20X1_1_PERSTN_M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

PCIe2.0 REFCLK



Note:

PCIE20_*_REFCLKP/N is output or input gpio

M*=Mean to M0 or M1 or M2,It's the same source,Just multiplex to M0 or M1 or M2,Only use one at the same time.

Note:

No PCIe for 12C project

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Page Name: 08.PCIE Fun Map

Size: A3 | Project Name: 12C_RK3588S | Rev: V1.0

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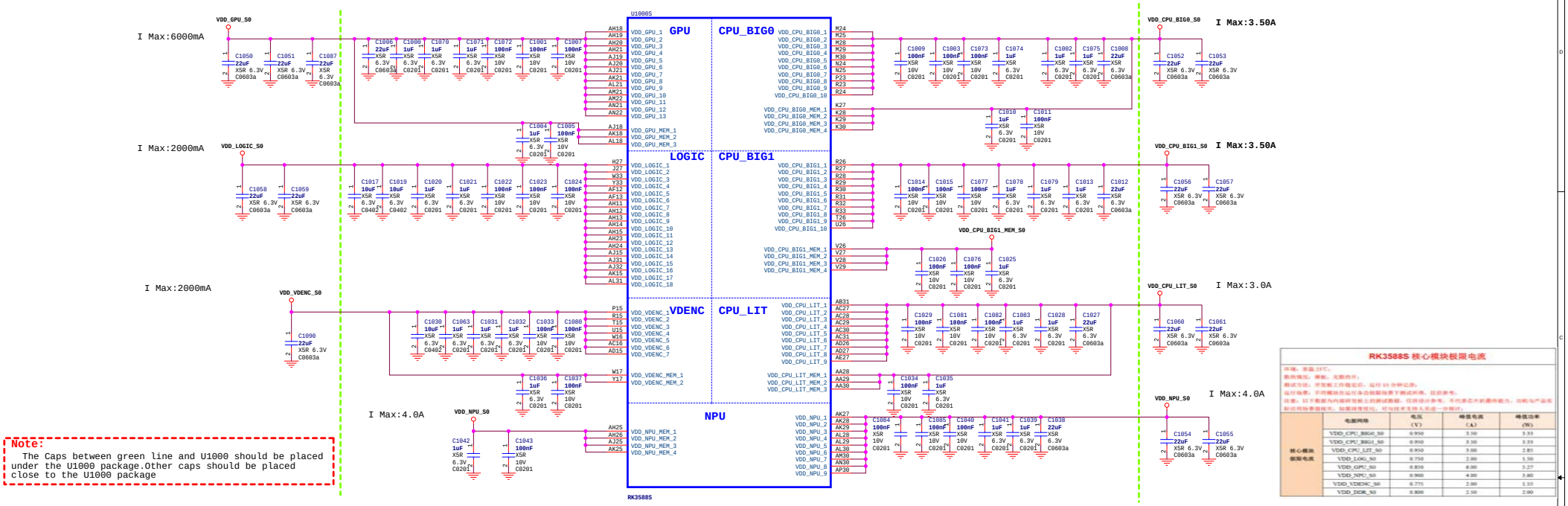
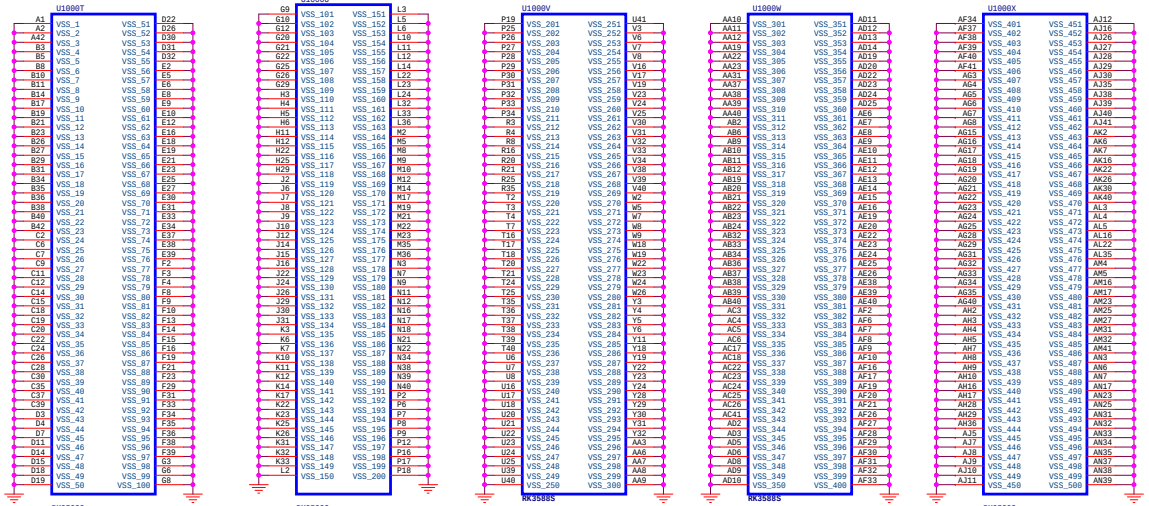
RK3588S(Power&Gnd)



Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package



RK3588S 核心模块板限电流

	电源网络	电压 (V)	峰值电流 (A)	峰值功率 (W)
核心模块板限电流	VDD_CPU_BIG0_S0	0.950	3.50	3.33
	VDD_CPU_BIG1_S0	0.950	3.50	3.33
	VDD_CPU_LIT_S0	0.950	3.00	2.85
	VDD_LOG_S0	0.750	2.00	1.50
	VDD_GPU_S0	0.850	6.00	5.27
	VDD_NPU_S0	0.900	4.00	3.60
	VDD_VDENC_S0	0.775	3.00	1.55
	VDD_DDR_S0	0.800	2.50	2.00

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Page Name: 10.RK3588S_Power/GND

Size: A2 | Project Name: 12C_RK3588S | Rev: V1.0

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RK3588S(OSC/PLL/PMUIO1)

Change Part

Note:
Adjusted the load capacitance according to the crystal specification

The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

CL={CL1*CL2/(CL1+CL2))}+PCB strays
Total CL<=12pF

Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package

U1000E RK3588S

OSC
XOUT_24M
XIN_24M

PLL
PLL_DVDD0V75
PLL_AVDD1V8
PLL_AVSS

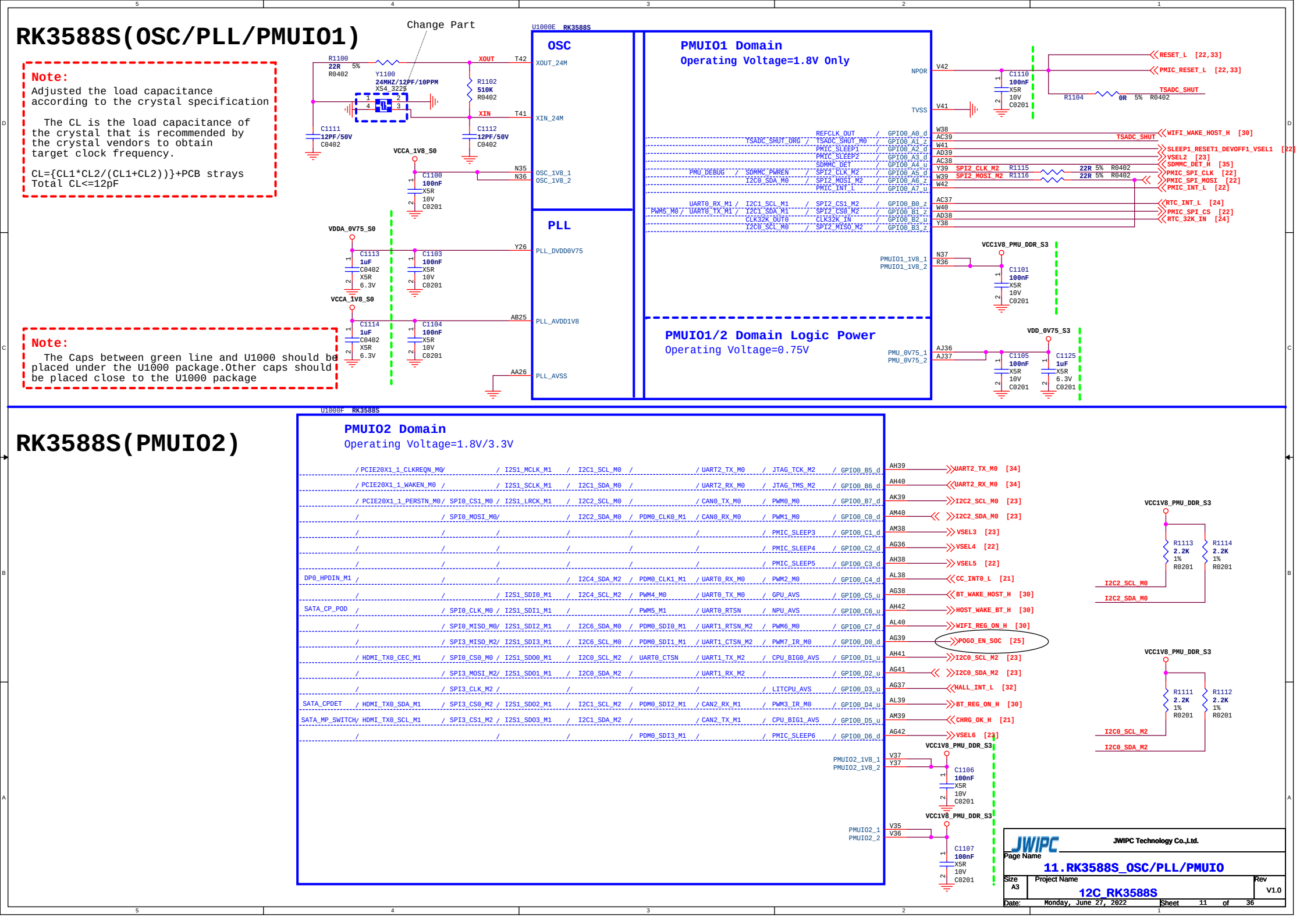
PMUIO1 Domain
Operating Voltage=1.8V Only

PMUIO1/2 Domain Logic Power
Operating Voltage=0.75V

RK3588S(PMUIO2)

U1000F RK3588S

PMUIO2 Domain
Operating Voltage=1.8V/3.3V



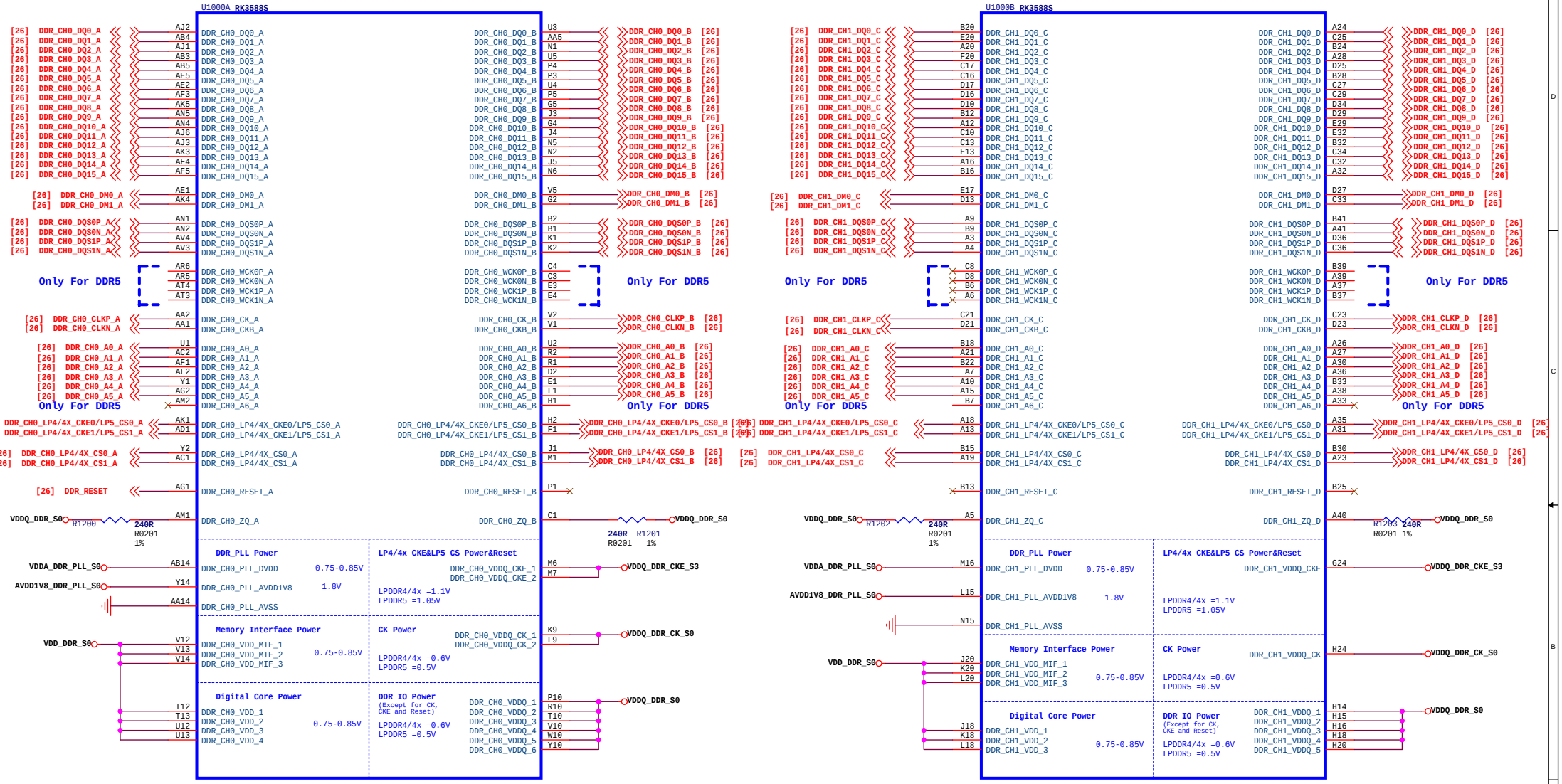
JWIPC Technology Co.,Ltd.

Page Name: 11.RK3588S_OSC/PLL/PMUIO

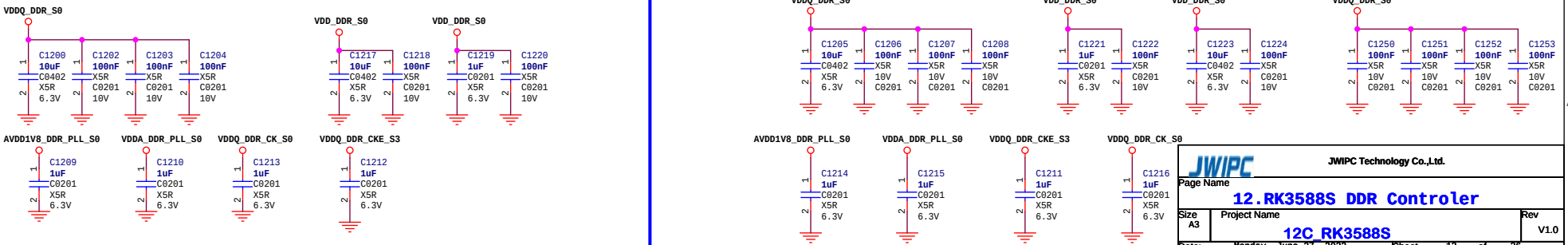
Size	Project Name	Rev
A3	12C_RK3588S	V1.0

Date: Monday, June 27, 2022 Sheet 11 of 36

RK3588S(DDR PHY)



DDR FILTER



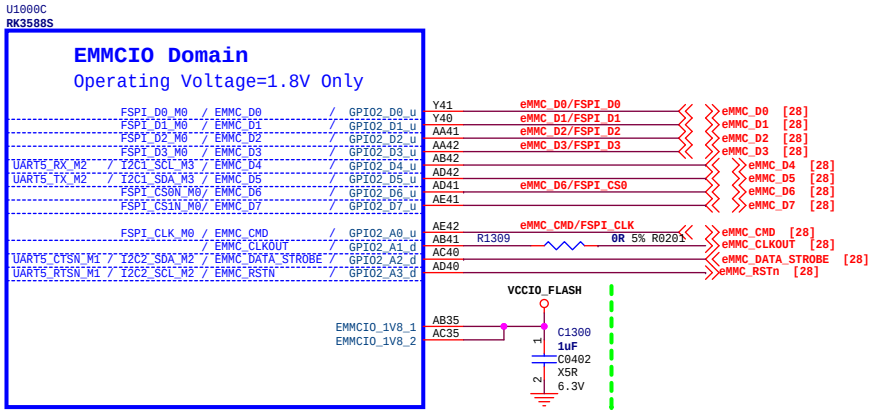
JWIPC Technology Co.,Ltd.

Page Name: 12.RK3588S DDR Controler

Size: A3 | Project Name: 12C_RK3588S | Rev: V1.0

Date: Monday, June 27, 2022 | Sheet 12 of 36

RK3588S(EMMCIO Domain)

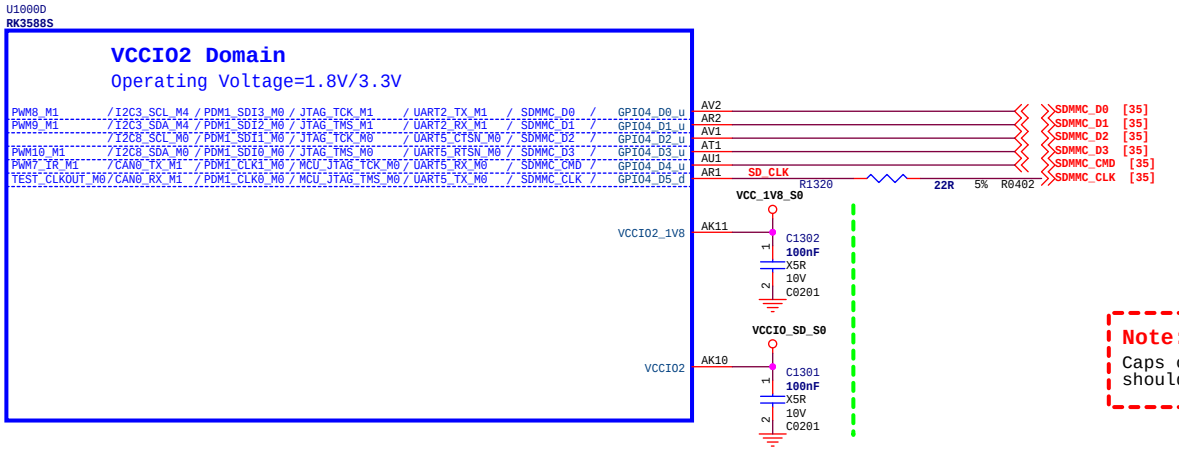


Default:eMMC

EMMC SINGLE Pair:
DATE:50 Ohm +-10%

Option:SPI Flash

RK3588S(VCCIO2 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

JWIPC Technology Co.,Ltd.

Page Name: 13.RK3588S Flash/SD Controller

Size	Project Name	Rev
A3	12C_RK3588S	V1.0

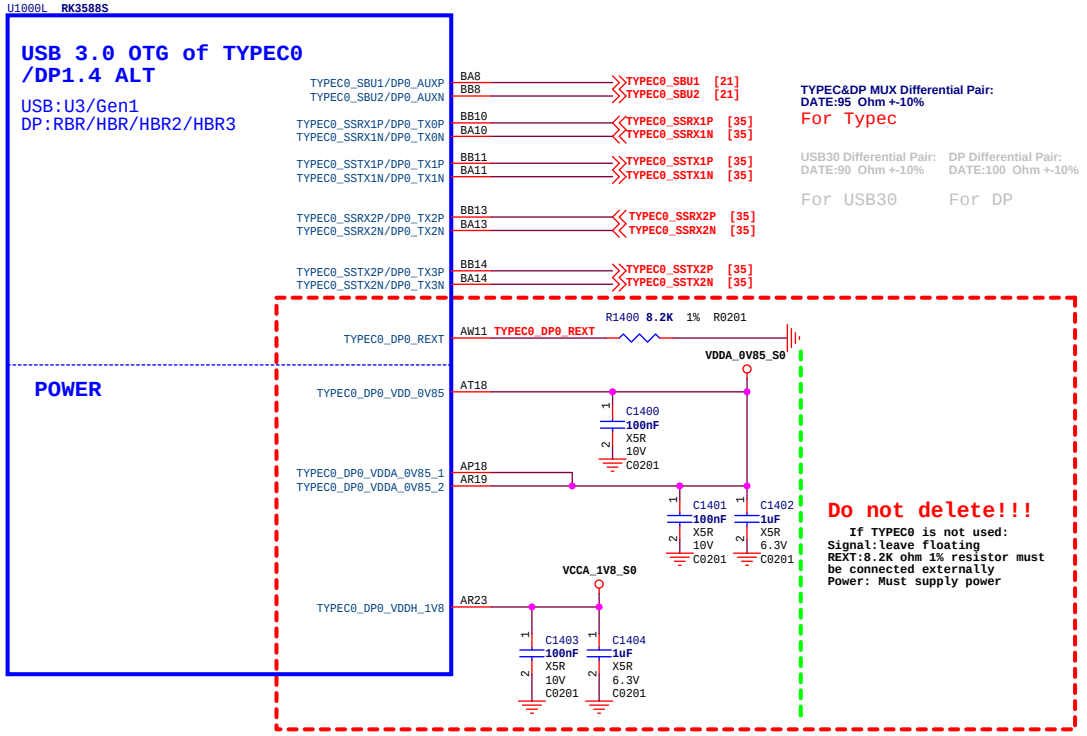
Date: Monday, June 27, 2022 Sheet 13 of 36

RK3588S(USB3.0/DP1.4)

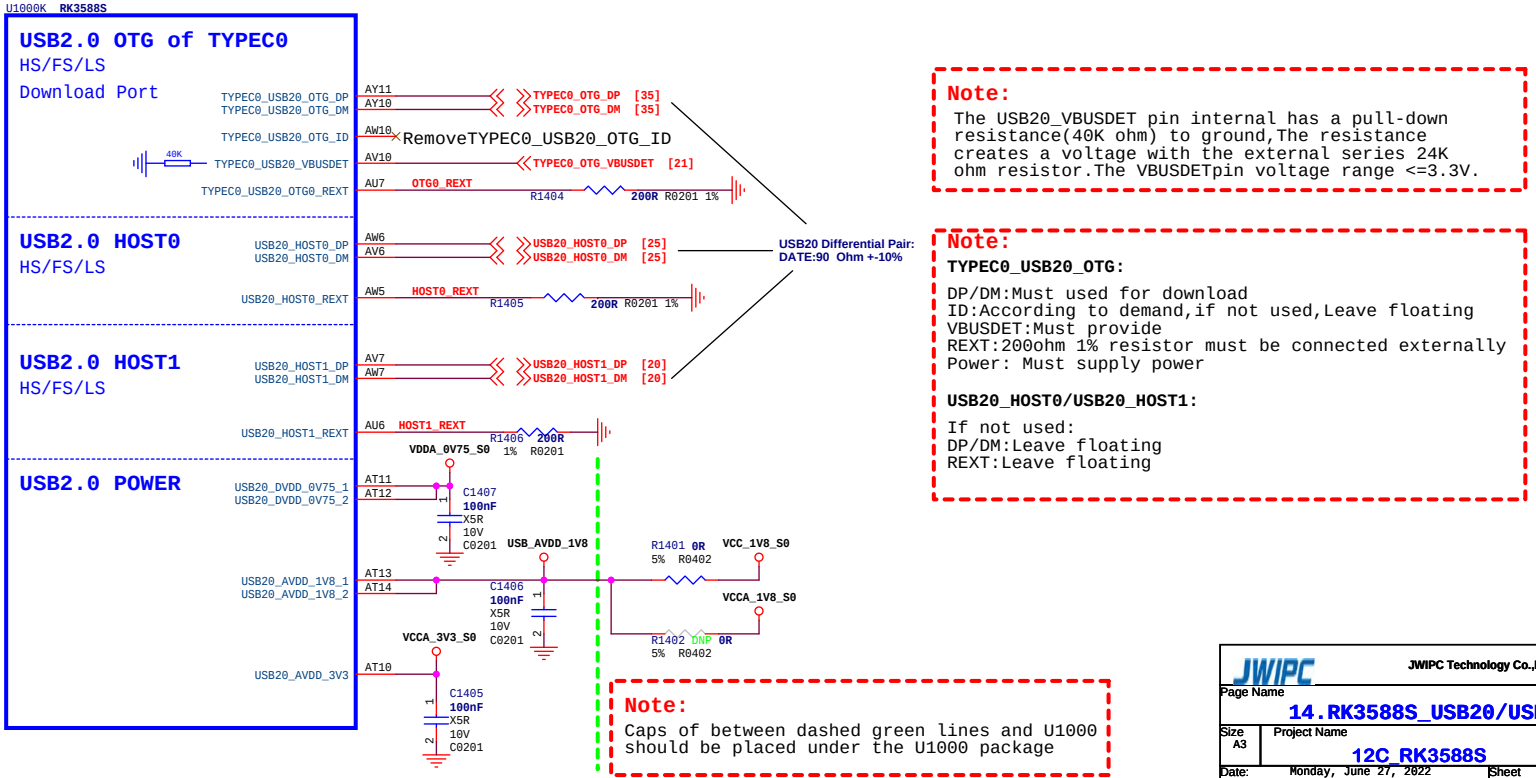
USB30/DP1.4 Alt Mode Configuration

Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*TYPEC x4Lane*	*SSTX 1P/1N SSTX 2P/2N SSRX 1P/1N SSRX 2P/2N*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:SSTX 1P/1N SSRX 1P/1N DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:SSTX 2P/2N SSRX 2P/2N DP:Lane0 Lane1*

DP Lane
Swap Off:
Lane0/1/2/3_TXdata mapping to Lane0/1/2/3_TXDP/N
Swap On:
Lane0/1/2/3_TXdata mapping to Lane2/3/0/1_TXDP/N



RK3588S(USB2.0)



Note:
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 24K ohm resistor.The VBUSDETpin voltage range <=3.3V.

Note:
TYPEC0_USB20_OTG:
DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power

USB20_HOST0/USB20_HOST1:
If not used:
DP/DM:Leave floating
REXT:Leave floating

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

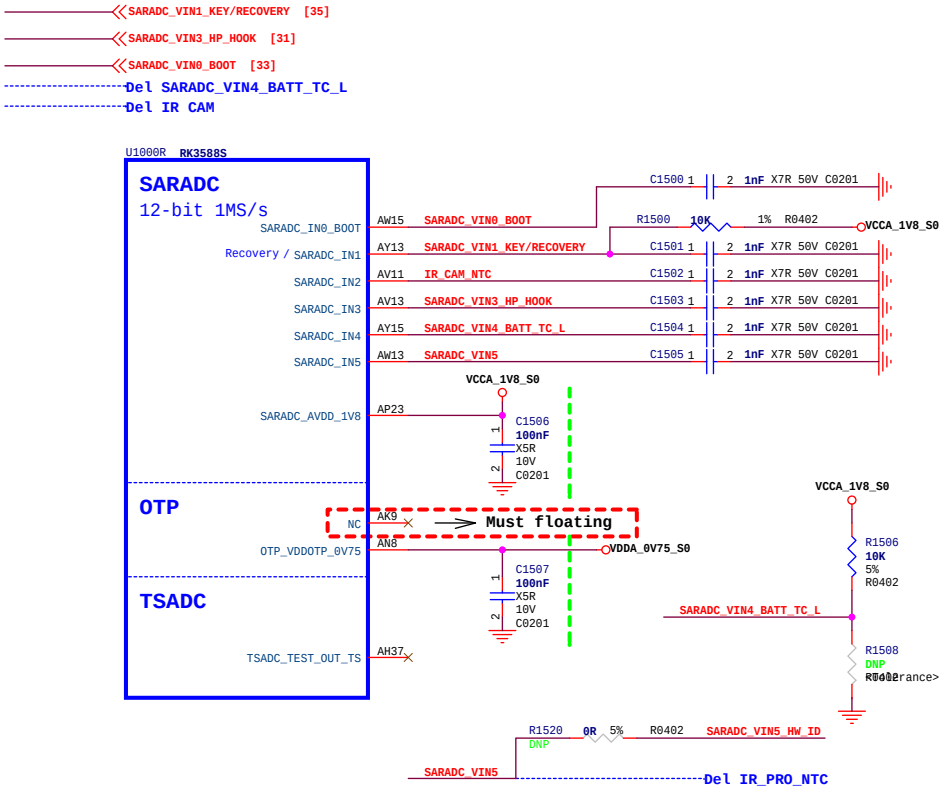
JWIPC Technology Co.,Ltd.

Page Name: 14.RK3588S_USB20/USB30/DP PHY

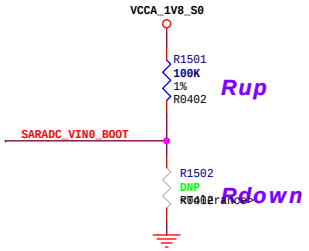
Size	Project Name	Rev
A3	12C_RK3588S	V1.0

Date: Monday, June 27, 2022 Sheet 14 of 36

RK3588S(SARADC/OTP/TSADC)

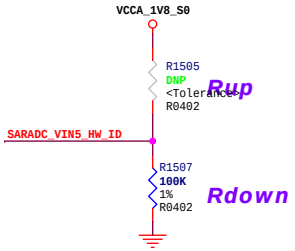


BOOT MODE CONFIG



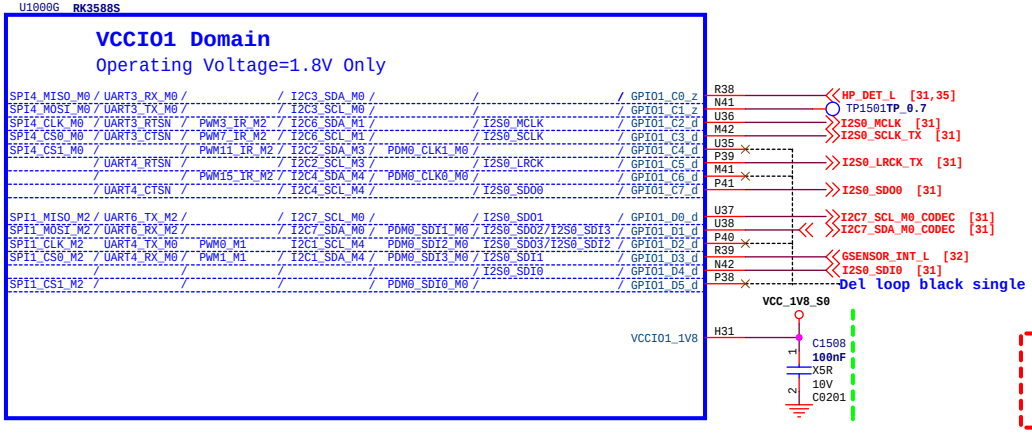
Item	Rup	Rdown	ADC	BOOT MODE(saradc_in5)
LEVEL1	DNP	100K	0	USB (Maskrom mode)
LEVEL2	100K	20K	682	SD Card-USB
LEVEL3	100K	51K	1365	EMMC-USB
LEVEL4	100K	100K	2047	FSPI M0-USB
LEVEL5	100K	200K	2730	FSPI M1-USB
LEVEL6	100K	499K	3412	FSPI M2-USB
LEVEL7	100K	DNP	4095	FSPI_M2-FSPI_M0-EMMC -SD Card-USB

BOARD ID CONFIG



Item	Rup	Rdown	ADC	VERSION
LEVEL1	DNP	100K	0	V1.0
LEVEL2	100K	20K	682	V2.0
LEVEL3	100K	51K	1365	V3.0
LEVEL4	100K	100K	2047	V4.0
LEVEL5	100K	200K	2730	V5.0
LEVEL6	100K	499K	3412	V6.0
LEVEL7	100K	DNP	4095	V7.0

RK3588S(VCCIO1 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

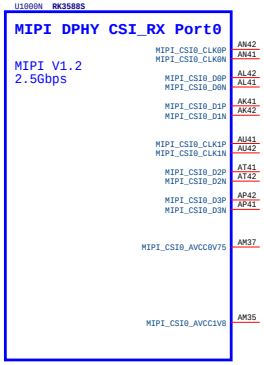
JWIPC Technology Co.,Ltd.

Page Name: 15.RK3588S_SARADC/1.8V GPIO

Size	Project Name	Rev
A3	12C_RK3588S	V1.0

Date: Monday, June 27, 2022 Sheet 15 of 36

RK3588S(MIPI_DPHY CSI0 RX)



MIPI CSI Differential Pair:
100 Ohm +-10%

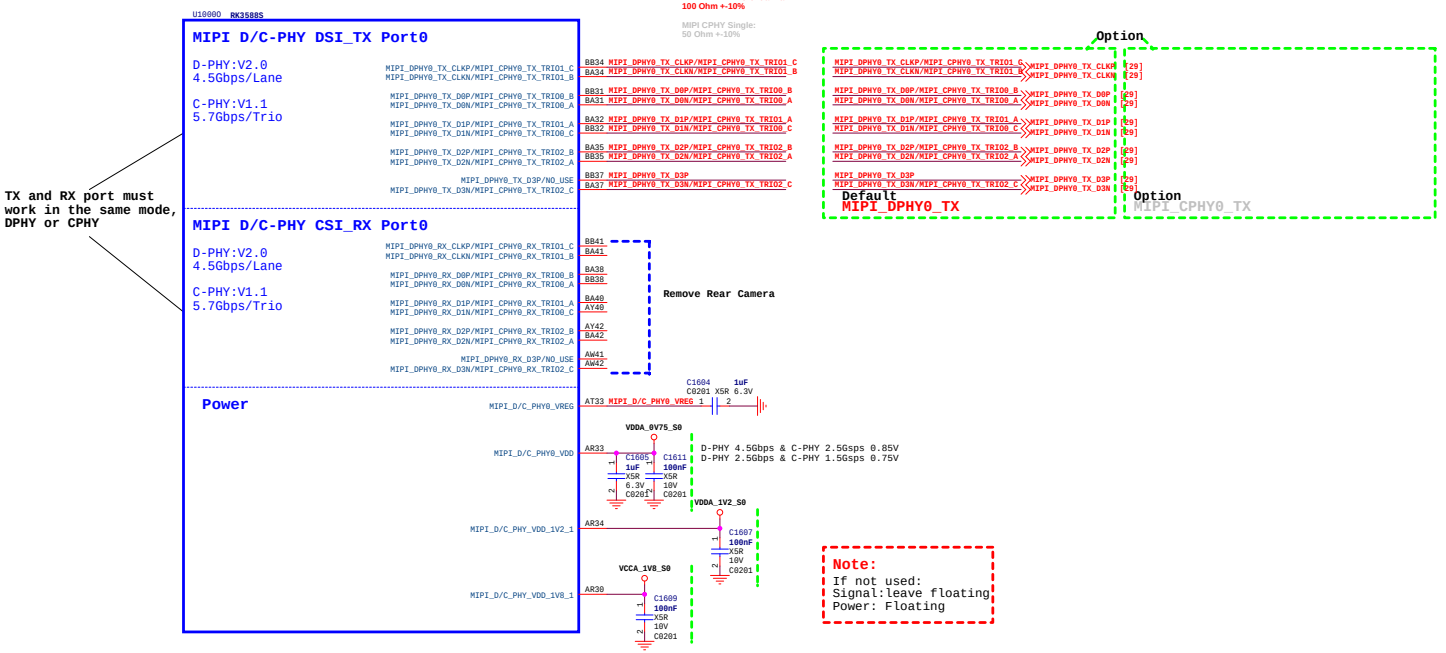
Note:
If not used:
Signal:leave floating
Power: Floating

Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane* + *Sensor2 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0* *MIPI_CSI_RX_D2-3* *MIPI_CSI_RX_CLK1*

Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3,but clock lane1 is invalid; In dual clock lanes mode,CLK0P/0N is the clock lane of Data lane0 and Data lane1,while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3588S(MIPI_D/C PHY0)

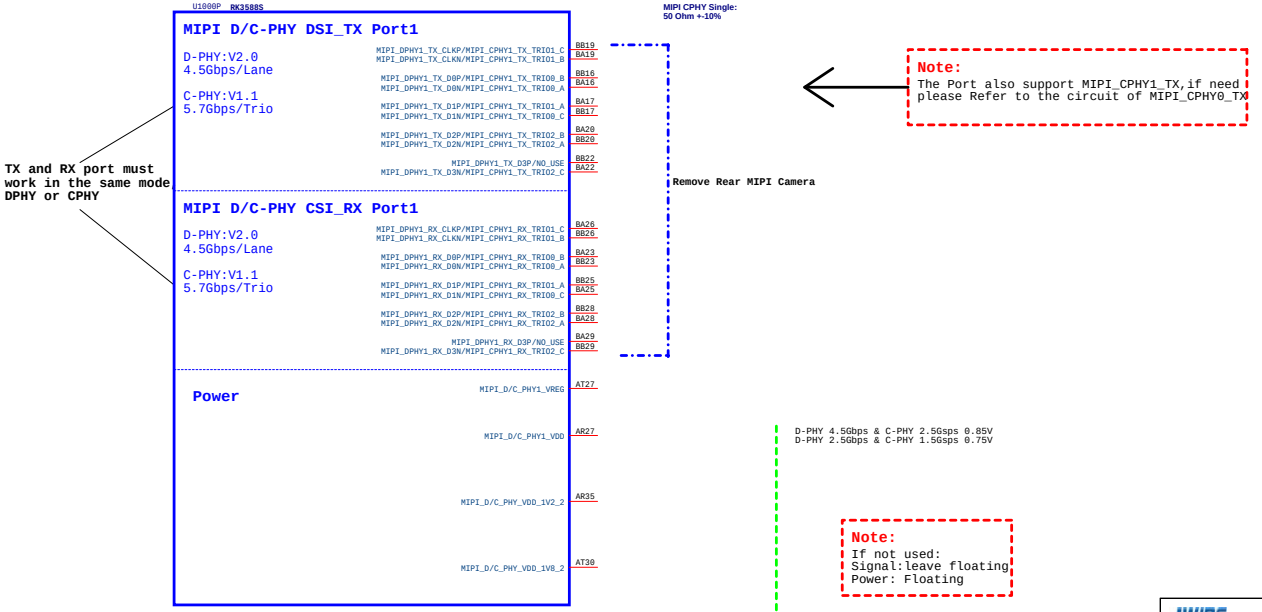


MIPI DPHY Differential Pair:
100 Ohm +-10%

MIPI CPHY Single:
50 Ohm +-10%

Note:
If not used:
Signal:leave floating
Power: Floating

RK3588S(MIPI_D/C PHY1)



MIPI DPHY Differential Pair:
100 Ohm +-10%

MIPI CPHY Single:
50 Ohm +-10%

Note:
The Port also support MIPI_CPHY1_TX,if need please Refer to the circuit of MIPI_CPHY0_TX

Note:
If not used:
Signal:leave floating
Power: Floating

JWIPC Technology Co.,Ltd.

Page Name: 16.RK3588S_MIPI Interface

Size: A2 | Project Name: 12C_RK3588S | Rev: V1.0

Date: Monday, June 27, 2022 | Sheet 16 of 36

RK3588S(HDMI2.1 TX/eDP1.3 TX)

Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.

U1000Q

HDMI TX/eDP1.3 MUX Port0

HDMI:V2.1 12Gbps
eDP: V1.3 5.4Gbps

HDMI_TX0_D0P/EDP_TX0_D0P	BB4
HDMI_TX0_D0N/EDP_TX0_D0N	BA4
HDMI_TX0_D1P/EDP_TX0_D1P	BA5
HDMI_TX0_D1N/EDP_TX0_D1N	BB5
HDMI_TX0_D2P/EDP_TX0_D2P	BB7
HDMI_TX0_D2N/EDP_TX0_D2N	BA7
HDMI_TX0_D3P/EDP_TX0_D3P	BA2
HDMI_TX0_D3N/EDP_TX0_D3N	BB2
HDMI_TX0_SBDP/EDP_TX0_AUXP	BA1
HDMI_TX0_SBDN/EDP_TX0_AUXN	AY1
HDMI/eDP_TX0_REXT	AY3

POWER

HDMI/EDP_TX0_VDD_0V75_1	AM13
HDMI/EDP_TX0_VDD_0V75_2	AN12
HDMI/EDP_TX0_AVDD_0V75	AN10
HDMI/EDP_TX0_VDD_IO_1V8	AK12
HDMI/EDP_TX0_VDD_CMN_1V8	AL14

RK3588S

Del HDMI2.1 TX/eDP1.3 TX

eDP TX
100 Ohm ±10%

HDMI TX
100 Ohm ±10%

Option

Option1:eDP_TX0

Option2:HDMI_TX0

Note:
If not used:
Signal:leave floating
Power: Floating or tie to VSS

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

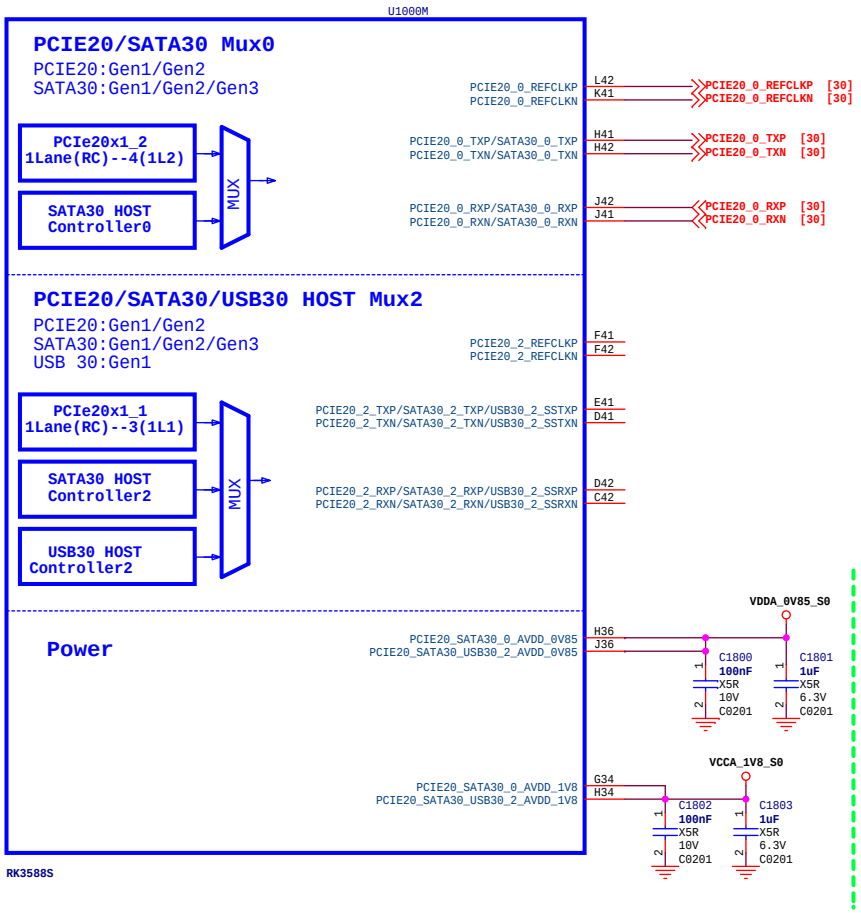
JWIPC Technology Co.,Ltd.

Page Name: 17.RK3588S_HDMI/eDP Interface

Size	Project Name	Rev
A4	12C_RK3588S	V1.0

Date: Monday, June 27, 2022 Sheet 17 of 36

RK3588S(PCIE20/SATA30/USB30)



CLK Differential Pair:
100 Ohm±10%
DATA Differential Pair:
PCIE20: 85 Ohm ±10%
SATA30: 100 Ohm ±10%
USB30: 90ohm ±10%

Note:
If not used:
Signal:leave floating
Power: Tie to VSS

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

PCIe2.0 PHY

Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ_M* PCIE20X1_1_WAKEN_M* PCIE20X1_1_PERSTN_M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

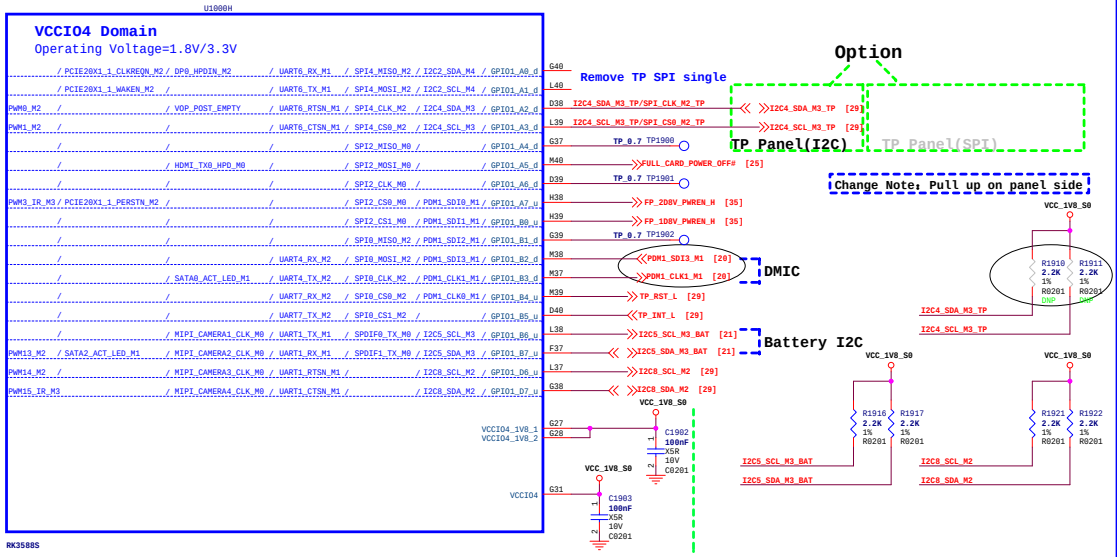
JWIPC Technology Co.,Ltd.

Page Name: 18.RK3588S PCIE2/SATA3/USB3 PHY

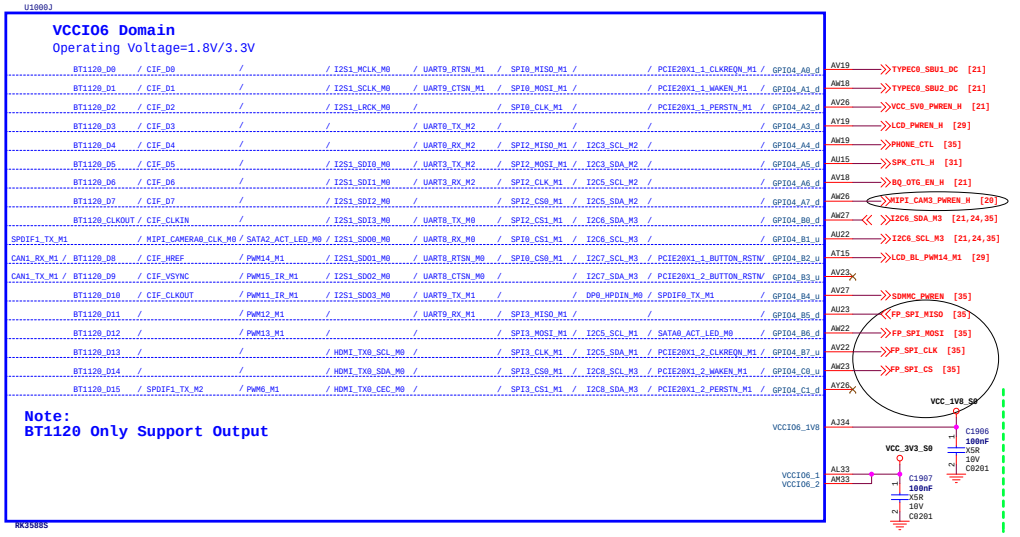
Size: A3 | Project Name: 12C_RK3588S | Rev: V1.0

Date: Monday, June 27, 2022 | Sheet 18 of 36

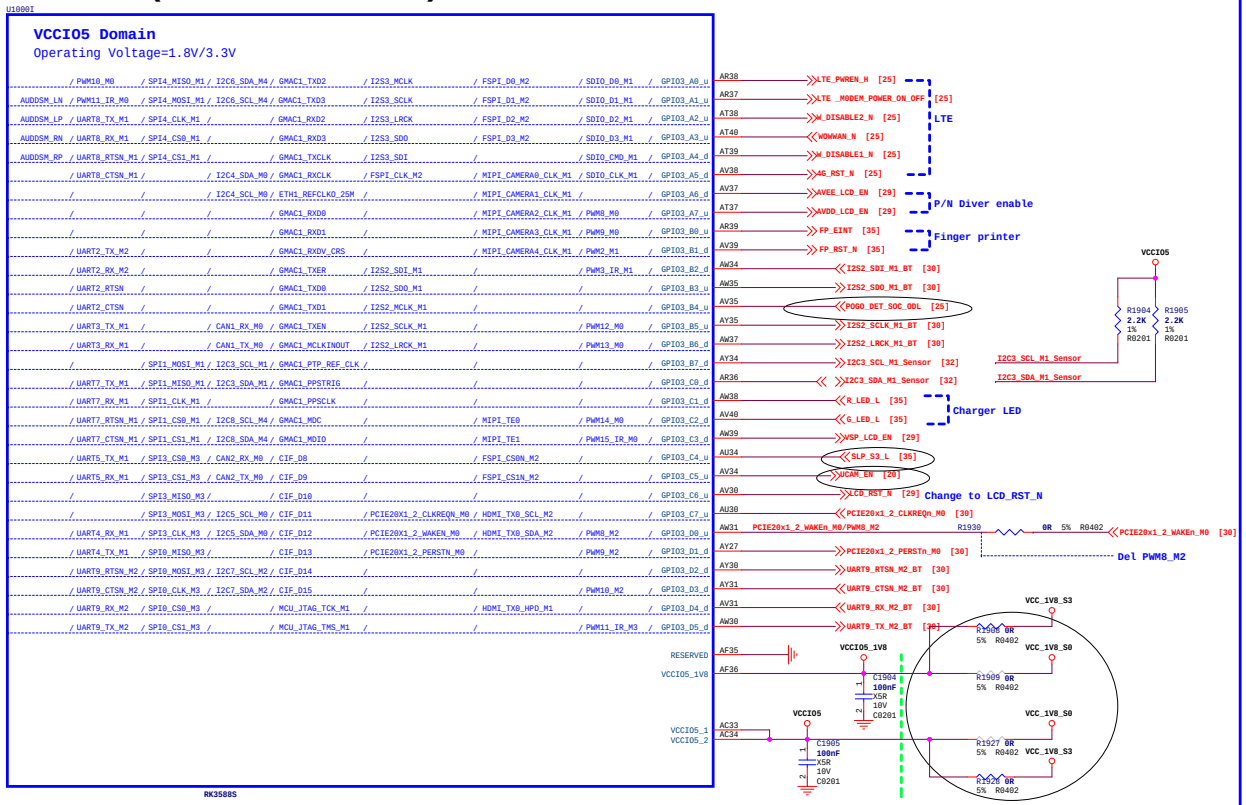
RK3588S(VCCIO4 Domain)



RK3588S(VCCIO6 Domain)



RK3588S(VCCIO5 Domain)

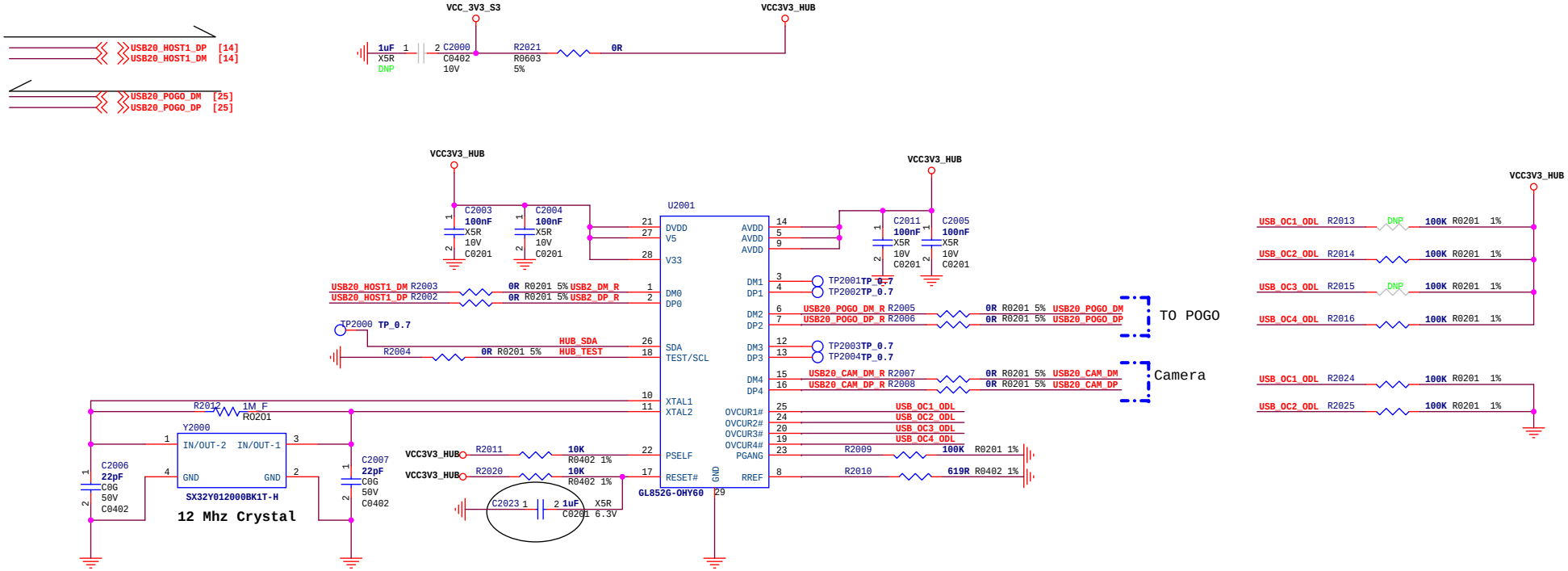


Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

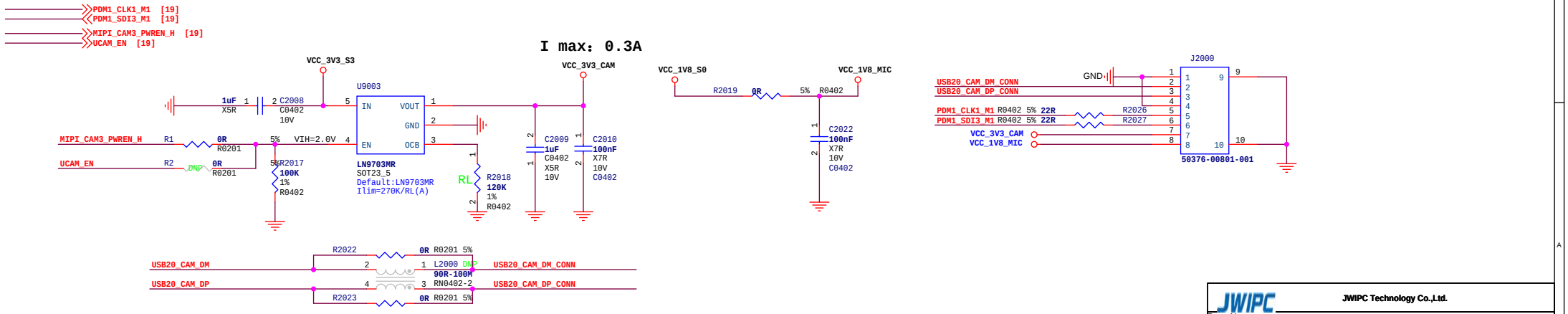
Change Note: VCCIO 5 power chang to S3, For Solve WIFI module S3 power Leakage issue!

JWIPC Technology Co.,Ltd.		
Page Name: 19.RK3588S GPIO		
Size: A2	Project Name: 12C_RK3588S	Rev: V1.0
Date: Thursday, June 30, 2022	Sheet 19 of 38	

USB 2.0 HUB



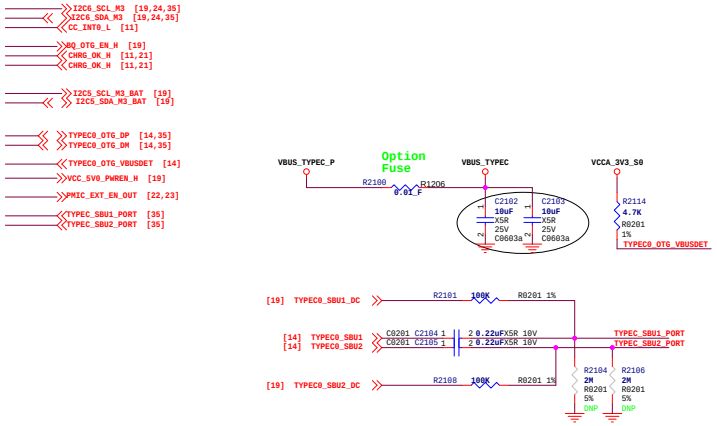
Front Camera combom with DMIC



JWIPC	JWIPC Technology Co.,Ltd.	
Page Name	20.USB2.0 HUB/CAM	
Size A3	Project Name 12C_RK3588S	Rev V1.0
Date: Monday, June 27, 2022	Sheet 20 of 36	

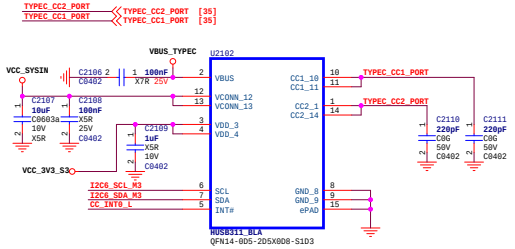
Power_3Cell_QC

USB Type-C Port Move TO DB



ESD

USB Type-C Controller(PD)

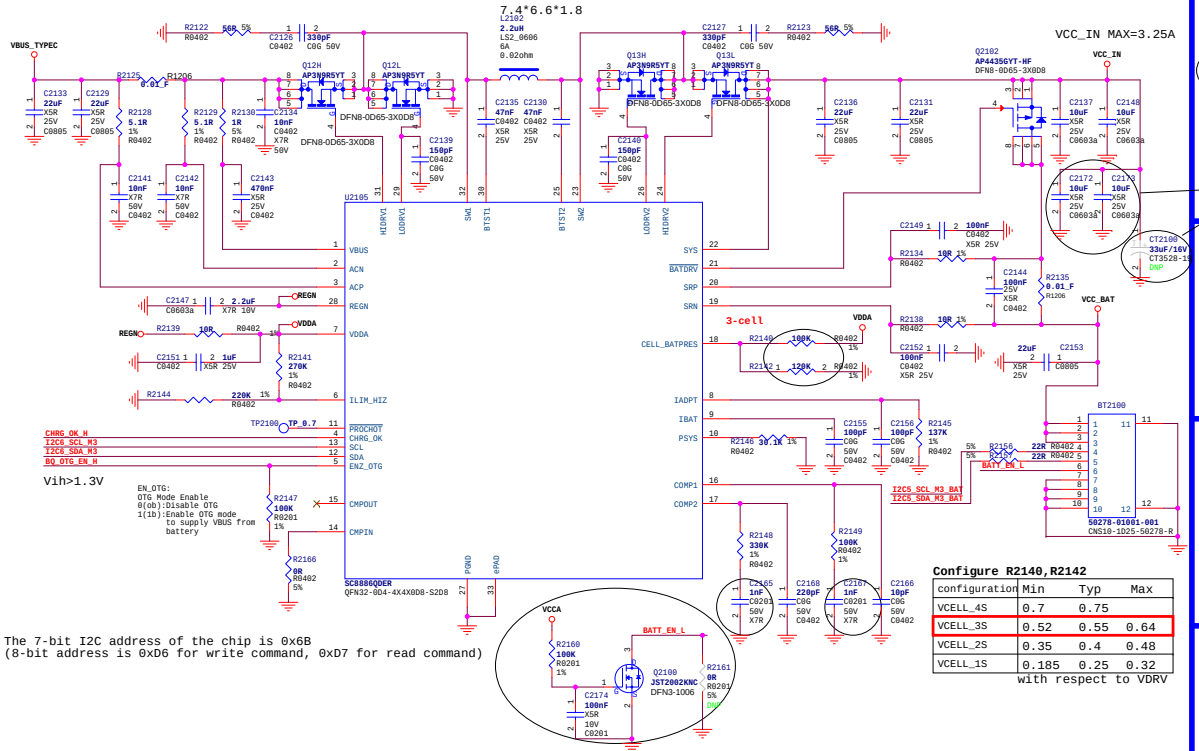


Dual Slave address=0x4E/0x3E
VBUS of HUSB311_BLA: 4 to 22V
VDD of HUSB311_BLA: 2.8 to 5.5V
VCONN of HUSB311_BLA: 2.4 to 5.3V

Gas Gauge

Charger IC

Change Note: Make Cap size more small for reduce acoustic noise



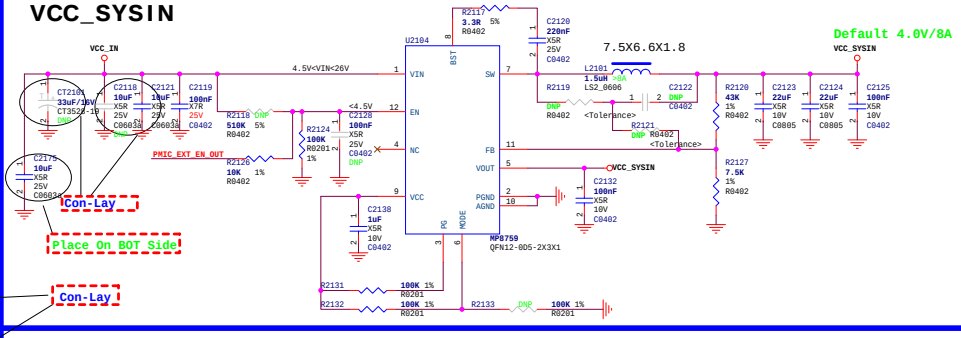
The 7-bit I2C address of the chip is 0x6B
(8-bit address is 0xD6 for write command, 0xD7 for read command)

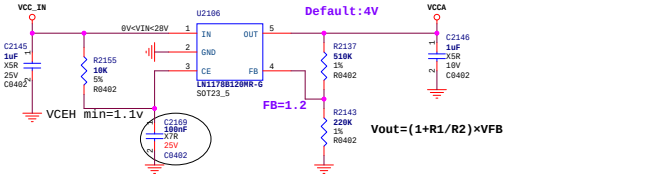
Configure R2140,R2142

configuration	Min	Typ	Max
VCELL_4S	0.7	0.75	
VCELL_3S	0.52	0.55	0.64
VCELL_2S	0.35	0.4	0.48
VCELL_1S	0.185	0.25	0.32

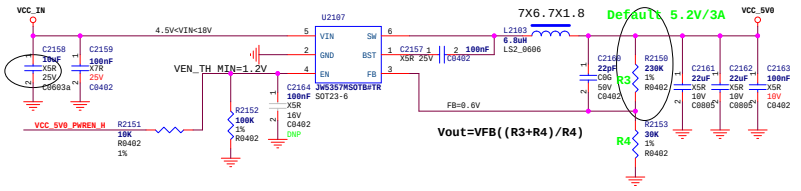
with respect to VDRV

VCC_SYSIN

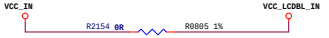




VCC_5V0



LCD Backlight power input source



JWIPC Technology Co.,Ltd.

Page Name: 21.Power_2Cell_QC(opt2)

Size	Project Name	Rev
A2	12C_RK3588S	V1.0

Date: Monday, June 27, 2022 Sheet 21 of 36

PMIC1 RK806-1

SLEEP1_RESET1_DEVOFF1_VSEL1 [11]
VSEL4 [11]
VSEL5 [11]
PMIC_INT_L [11]
PWRON_L [35]
PMIC_RESET_L [11,33]
PMIC_EXT_EN_OUT [21,23]
PMIC_SPI_CLK [11]
PMIC_SPI_CS [11]
PMIC_SPI_MOSI [11]

VCC_SYSIN
ED2200 AZ5725-01F DFN2-1006

IF TVS UNMOUNTED, ESD OR SURGE SHOULD BE DAMAGE THE PMIC!!!

This device must be mounted.Replacing TVS mode is not recommended, if must, please choose the same specifications
Operating Supply Vtage : 5.5V(5.25-6V)
PeakPulse Current: >10A (tp=8/20uS)
Surge Clamping Voltage: <6.5V

DO NOT DELETE IT!

VSEL5 — R2242 0R 5% R0402 — PMIC_PWR_CTRL2

VSEL4 — R2290 0R 5% R0402 — PMIC_PWR_CTRL3

PMIC RK806-1 BUCK

U2200A

BUCK5 2.5A — I Max:2.50A
VDD_DDR_S0
Default:0.85V
Low frequency: 0.85V-->0.75V
C2200 22uF X5R 10V C0603a
L2200 0.47uH L2016-1d2H
PMIC_SW5
C2202 22uF X5R 6.3V C0603a
C2203 22uF X5R 6.3V C0603a
R2200 100R 5% R0402
C2266 1uF C0402 X5R 6.3V
VDD_DDR_S0 Feedback from RK3588S
FB5 (FB=0.5V)

BUCK1 6.5A — I Max:6.0A
C2201 22uF X5R 10V C0603a
L2201 0.22uH L2520-1d2H
PMIC_SW1
PMIC_VOUT1
VDD_GPU_S0
C2209 1uF C0402 X5R 6.3V
R2208 100R 5% R0402
C2210 47uF X5R 6.3V C0603a
C2205 47uF X5R 6.3V C0603a
C2280 22uF X5R 6.3V C0603a
VDD_GPU_S0 Feedback from RK3588S
(FB=0.5V) FB1

BUCK6 2.5A — I Max:3.0A
VDD2_DDR_S3
C2214 22uF X5R 6.3V C0603a
C2215 22uF X5R 6.3V C0603a
C2216 100pF C0G 50V C0402
L2202 0.47uH L2016-1d2H
PMIC_SW6
PMIC_VOUT6
R2218 120K 1% R0402
R2227 100K 1% R0402
FB6 (FB=0.5V)

LPDDR4/4x=1.1V	120K
LPDDR5=1.05V	110K

BUCK2 5A
C2213 22uF X5R 10V C0603a
L2203 0.24uH L2520-1d2H
PMIC_SW2
PMIC_VOUT2
VDD_CPU_LIT_S0
C2221 1uF C0402 X5R 6.3V
R2219 100R 5% R0402
C2217 22uF X5R 6.3V C0603a
C2218 22uF X5R 6.3V C0603a
C2219 22uF X5R 6.3V C0603a
VDD_CPU_LIT_S0 Feedback from RK3588S
(FB=0.5V) FB2

BUCK9 2.5A — I Max:2.50A
VDDQ_DDR_S0
C2225 10uF C0603a X5R 10V
C2228 22uF X5R 6.3V C0603a
C2227 22uF X5R 6.3V C0603a
C2229 100pF C0G 50V C0402
L2204 0.47uH L2016-1d2H
PMIC_SW9
PMIC_VOUT9
R2236 20K 1% R0402
R2241 100K 1% R0402
FB9 (FB=0.5V)

LPDDR4/4x=0.6V	20K	100K
LPDDR5=0.5V	0R	DNP

BUCK3 5A — I Max:2.0A
C2226 22uF C0603a X5R 10V
L2205 0.24uH L2520-1d2H
PMIC_SW3
VDD_LOGIC_S0
C2230 1uF C0402 X5R 6.3V
R2238 100R 5% R0402
C2231 22uF X5R 6.3V C0603a
C2232 22uF X5R 6.3V C0603a
C2282 22uF X5R 6.3V C0603a
Feedback from RK3588S

BUCK8 2.5A — I Max:2.50A
VCC_3V3_S3
C2238 22uF X5R 6.3V C0603a
C2239 22uF X5R 6.3V C0603a
L2206 0.47uH L2016-1d2H
PMIC_SW8
PMIC_VOUT8
VCC1V8_PMU_DDR_S3
VCC_1V8_S3_PLDO6
R2210 0R R0603 5% DNP
R2211 0R R0603 5%
Default:1.8V

BUCK4 5A — I Max:2.0A
C2236 22uF C0603a X5R 10V
L2207 0.24uH L2520-1d2H
PMIC_SW4
VDD_VDENC_S0
C2291 1uF C0402 X5R 6.3V
R2209 100R 5% R0402
C2240 22uF X5R 6.3V C0603a
C2237 22uF X5R 6.3V C0603a
C2283 22uF X5R 6.3V C0603a
Feedback from RK3588

BUCK10 2.5A
C2241 22uF C0603a X5R 10V
L2208 0.47uH L2016-1d2H
PMIC_SW10
PMIC_VOUT10
VCC_1V8_S3
C2242 22uF X5R 6.3V C0603a
C2243 22uF X5R 6.3V C0603a

BUCK7 2.5A — I Max:1.1A
L2209 0.47uH L2016-1d2H
PMIC_SW7
PMIC_VOUT7
VCC_2V0_PLDO_S3
C2244 22uF X5R 6.3V C0603a
C2245 22uF X5R 6.3V C0603a

RK806-1

PMIC RK806-1 Managerment

U2200C

VBUS_TYPEC
R2266 10K R0201 5%
C2267 10uF X5R 25V C0603a
R2264 10K R0201 5%
R2265 22K R0402
PMIC_VDC
D2600 BZT52C3V3S SOD323
C2260 1nF C0201 X7R 50V
C2261 100nF X5R 10V C0201
PWRON_L

VCC_1V8_S3_PLDO6
C2248 1uF C0402 X5R 6.3V
VCCA
C2254 1uF C0402 X5R 6.3V

VCCIO
(IIC/SPI)CS — PMIC_SPI_CS
(SDA)MOSI — PMIC_SPI_MOSI
(SCL)CLK — PMIC_SPI_CLK
(PWRCTRL3)SO — PMIC_PWR_CTRL3
PWRCTRL2 — PMIC_PWR_CTRL2
PWRCTRL1 — SLEEP1_RESET1_DEVOFF1_VSEL1
R2258 100K R0201 1%

VCCA
SYNC_CLK
SYNC
VDC
PWRON
(M/S)EXT_EN — PMIC_EXT_EN_OUT
INT — PMIC_INT_L
RESETB — PMIC_RESET_L
ePAD
R2261 10K R0402 1%
R2263 10K R0402 1%
C2262 100nF X5R 10V C0201

RK806-1

Change Note: Add RC For auto boot up when plug in AC

RK3588S nPOR
TSADC_SHUT
RK806-1 RESETB
Reset Key

Note:
- Reset Key Control Path
- TSADC_SHUT Control Path
- RK806-1 Control Path

PMIC RK806-1 LDO

U2200B

VCC_2V0_PLDO_S3
C2247 1uF X5R C0402 6.3V
VCC_SYSIN
C2252 1uF X5R C0402 10V
VCC_1V1_NLDO_S3
C2257 1uF X5R C0402 6.3V
VCC_1V1_NLDO_S3
C2264 1uF X5R C0402 6.3V

PLDO
VCC11 — 0.5A
VCC12 — 0.5A / 0.3A / 0.3A
PLDO1 — VCC_1V8_S0 — C2246 1uF C0402 X5R 6.3V — Default:1.8V
PLDO2 — VCCA_1V8_S0 — C2249 1uF C0402 X5R 6.3V — Default:1.8V
PLDO3 — VDDA_1V2_S0 — C2250 1uF C0402 X5R 6.3V — Default:1.2V
PLDO4 — VCCA_3V3_S0 — C2251 1uF C0402 X5R 6.3V — Default:3.3V
PLDO5 — VCCIO_SD_S0 — C2253 1uF C0402 X5R 6.3V — Default:3.3V

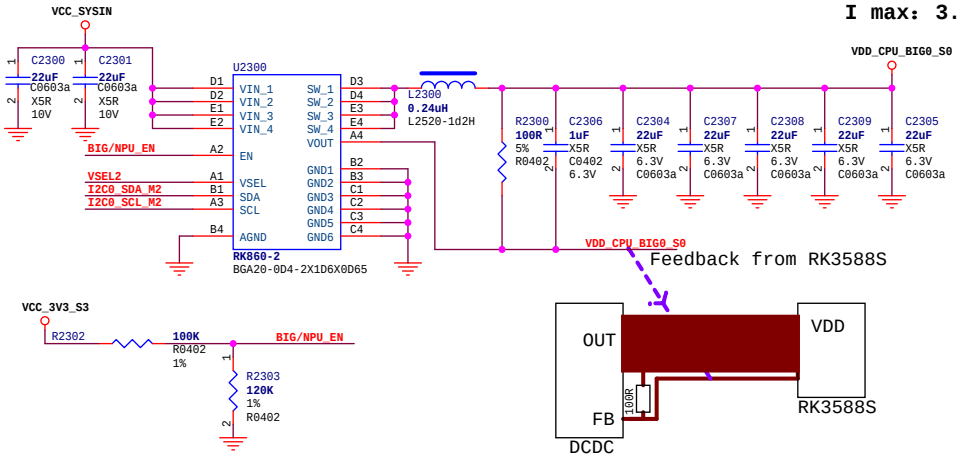
NLDO
VCC13 — 0.3A / 0.3A / 0.5A
VCC14 — 0.5A / 0.3A
NLDO1 — VDD_0V75_S3 — C2255 2.2uF 6.3VC0402 X5R — Default:0.75V
NLDO2 — VDDA_DDR_PLL_S0 — C2258 2.2uF 6.3VC0402 X5R — Default:0.85V; Low frequency:0.85V-->0.75V
NLDO3 — VDDA_0V75_S0 — C2259 2.2uF 6.3VC0402 X5R — Default:0.75V
NLDO4 — VDDA_0V85_S0 — C2263 2.2uF 6.3VC0402 X5R — Default:0.85V
NLDO5 — C2265 2.2uF 6.3VC0402 X5R — Default:0.75V Reserved

RK806-1

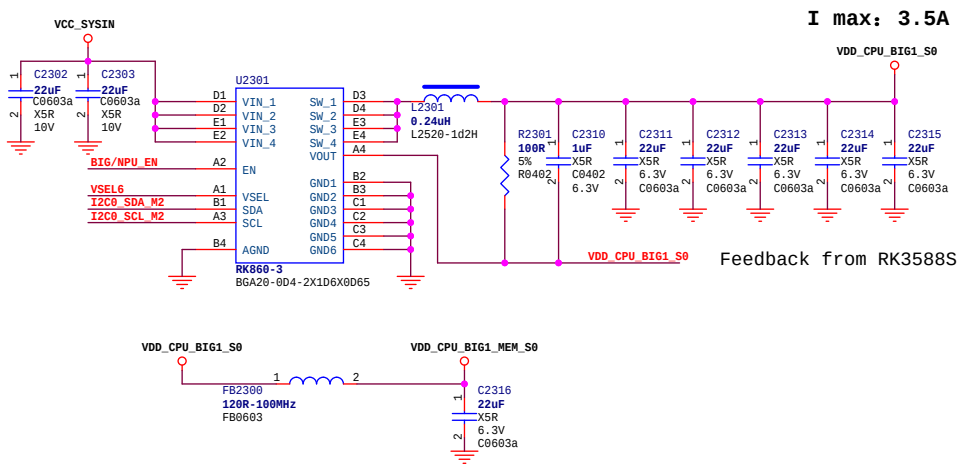
VCCA_1V8_S0 — R2274 0R R0402 5% — AVDD1V8_DDR_PLL_S0 — C2290 1uF X5R C0402 6.3V

JWIPC Technology Co.,Ltd.
Page Name: 22.Power-PMIC_RK806-1
Size: C | Project Name: 12C_RK3588S | Rev: V1.0
Date: Monday, June 27, 2022 | Sheet 22 of 36

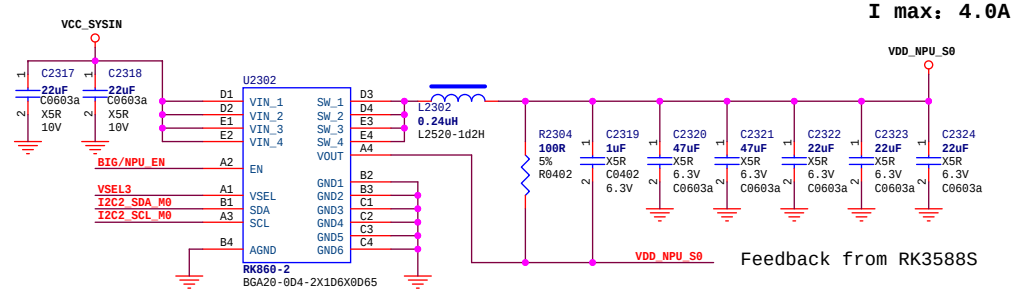
VDD_CPU_BIG0



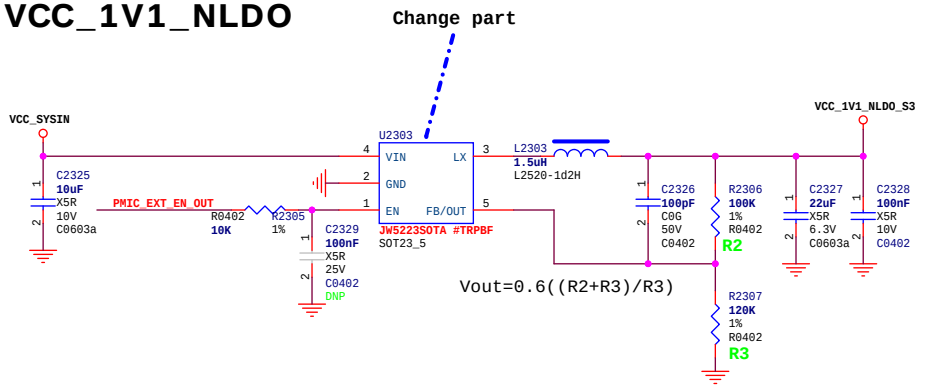
VDD_CPU_BIG1



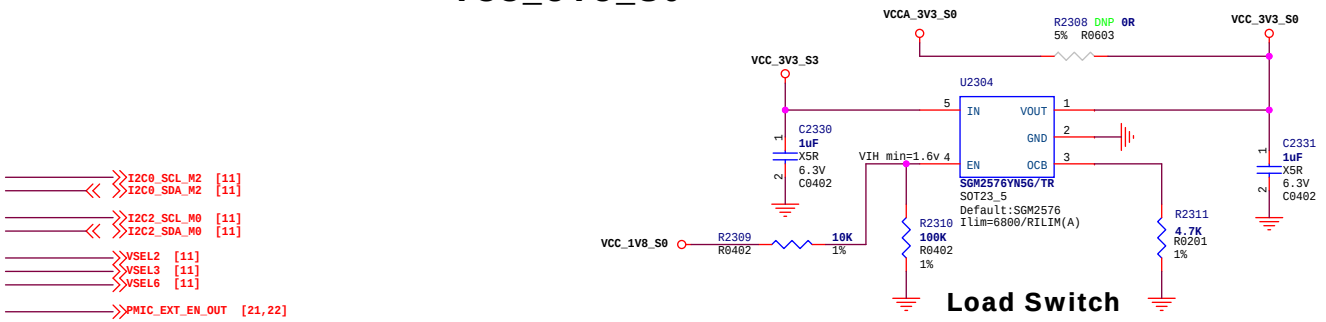
VDD_NPU



VCC_1V1_NLDO



VCC_3V3_S0

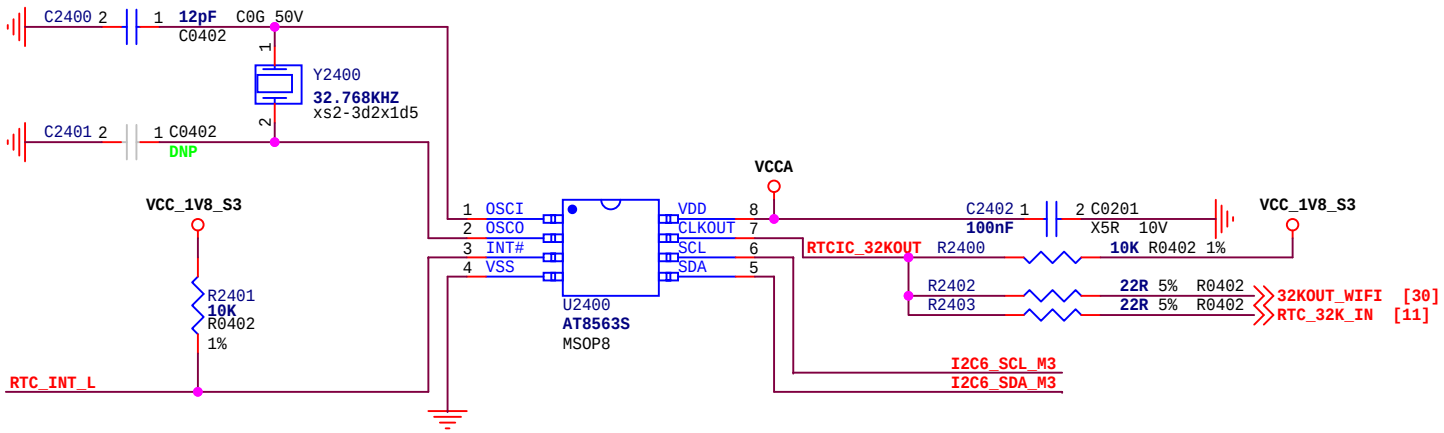


JWIPC Technology Co.,Ltd.		
Page Name: 23.Power_Ext Discrete		
Size: A3	Project Name: 12C_RK3588S	Rev: V1.0
Date: Monday, June 27, 2022	Sheet 23 of 36	

RTC IC

I2C6_SDA_M3 [19,21,35]
I2C6_SCL_M3 [19,21,35]

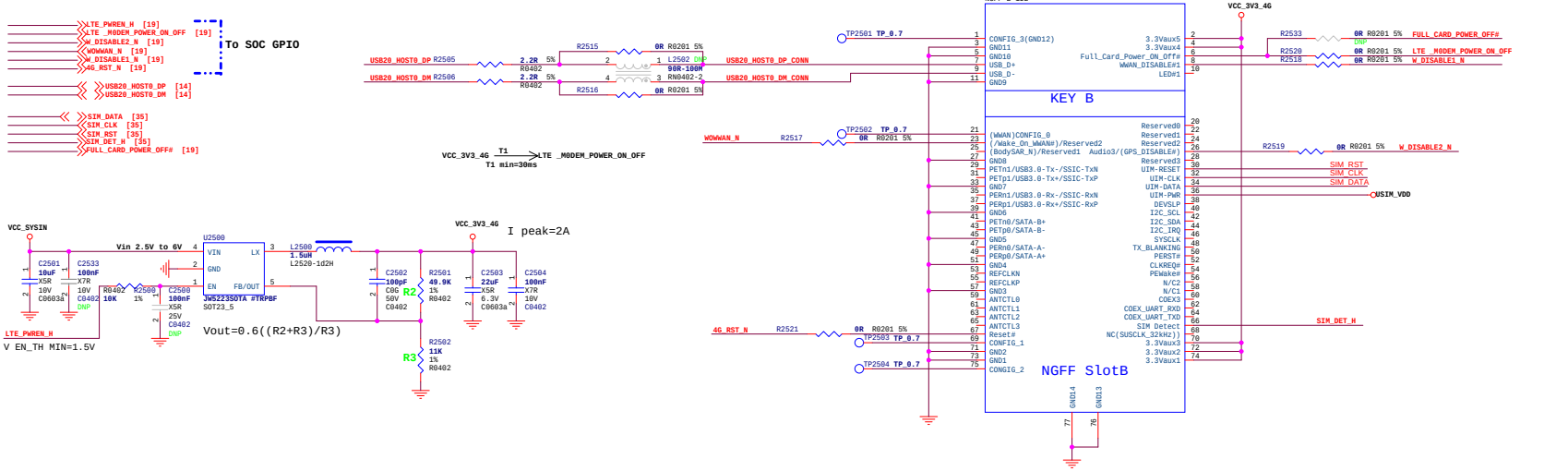
RTC_INT_L [11]



Address:Read A3H,Write A2H
Fscl=400kHz

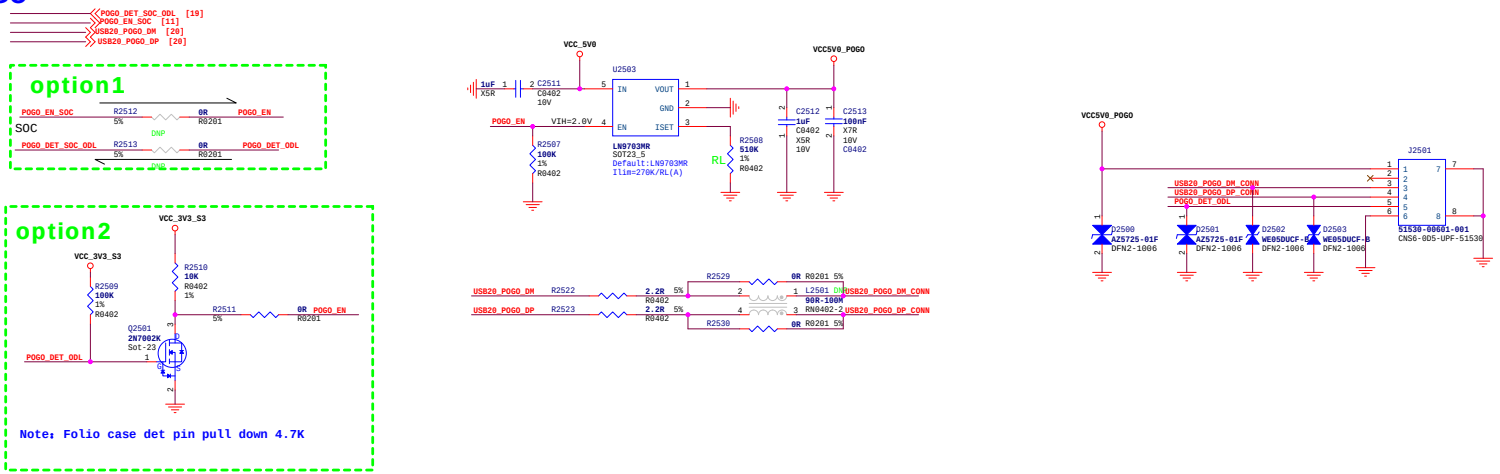
JWIPC	JWIPC Technology Co.,Ltd.	
Page Name	24.RTC	
Size A4	Project Name 12C_RK3588S	Rev V1.0
Date: Monday, June 27, 2022	Sheet 24 of 36	

USB2.0 MINI PCIe LTE



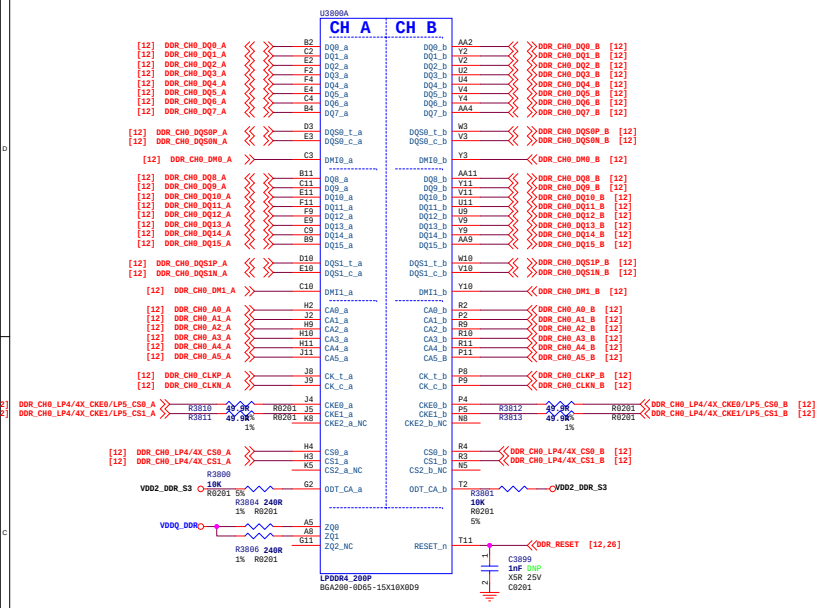
Fingerprint move to DB

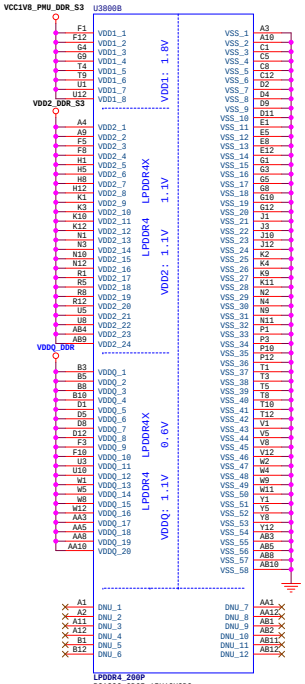
USB2.0 POGO

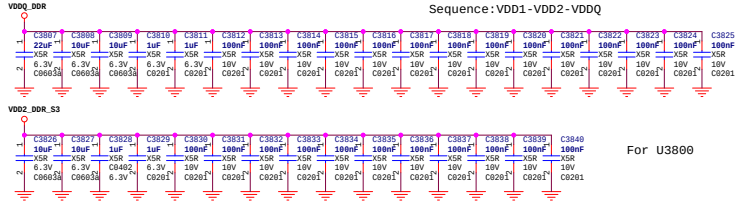


JWIPC Technology Co.,Ltd.		
Page Name	25.USB20/USB30 HOST Port	
Size A2	Project Name 12C RK3588S	Rev V1.0
Date: Monday, June 27, 2022	Sheet 25 of 38	

DRAM-LPDDR4/4x_2X32bit

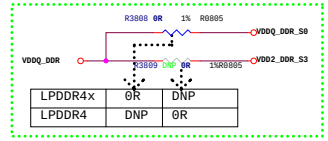




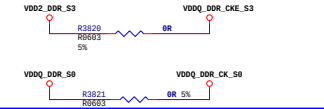


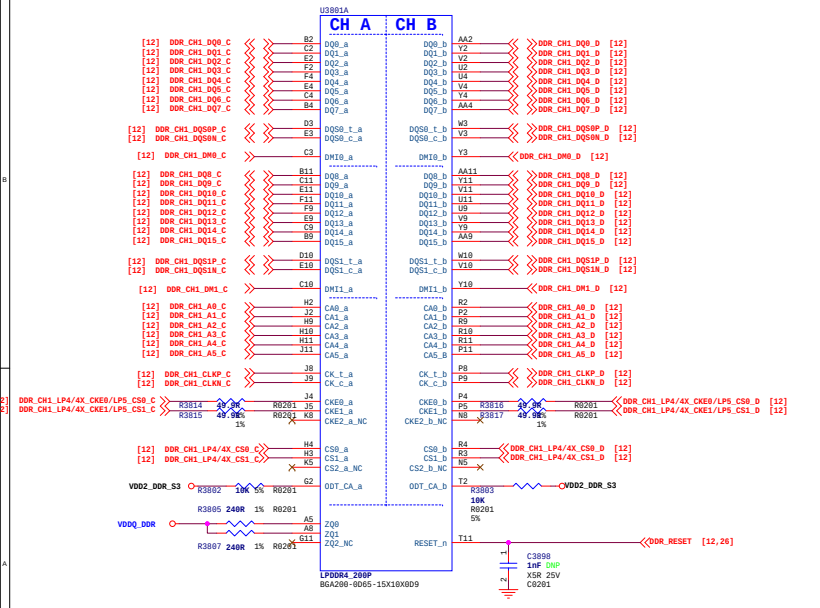
Sequence:VDD1-VDD2-VDDQ

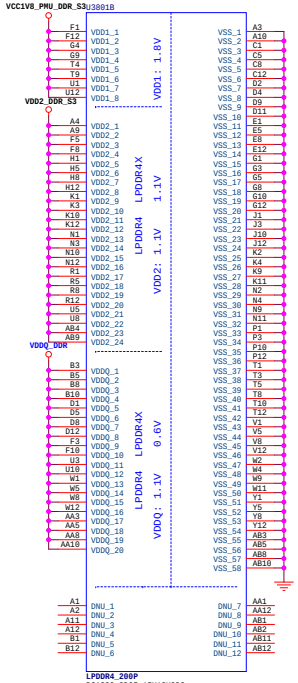
	LPDDR4	LPDDR4X
VDD1:	1.70-1.95	1.70-1.95
VDD2:	1.06-1.17	1.06-1.17
VDDQ:	1.06-1.17	0.57-0.65

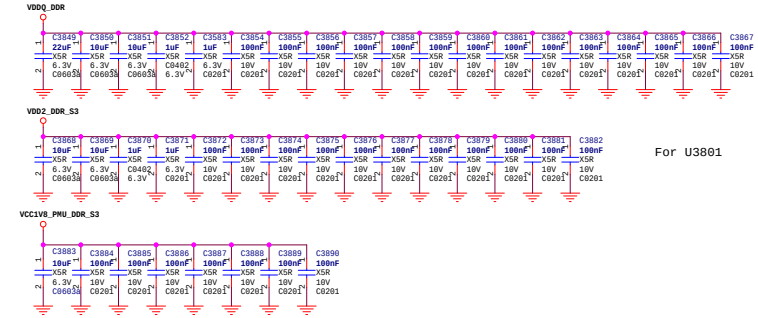


LPDDR4x	0R	DNP
LPDDR4	DNP	0R



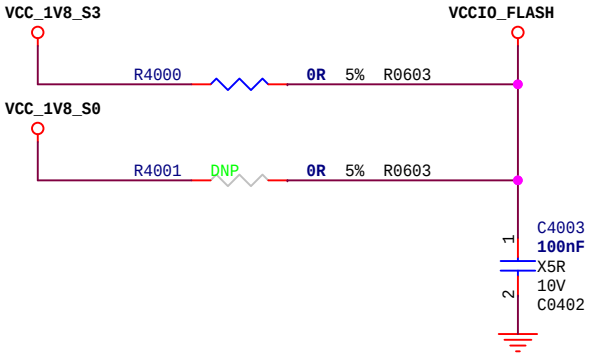






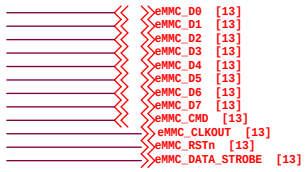
JWIPC	JWIPC Technology Co.,Ltd.
Page Name	26.DRAM-LPDDR4/4X_200P_2X32bit
Size: A2	Project Name: 12C RK3588S
Rev	V1.0
Date:	Monday, June 27, 2022
Sheet	26 of 36

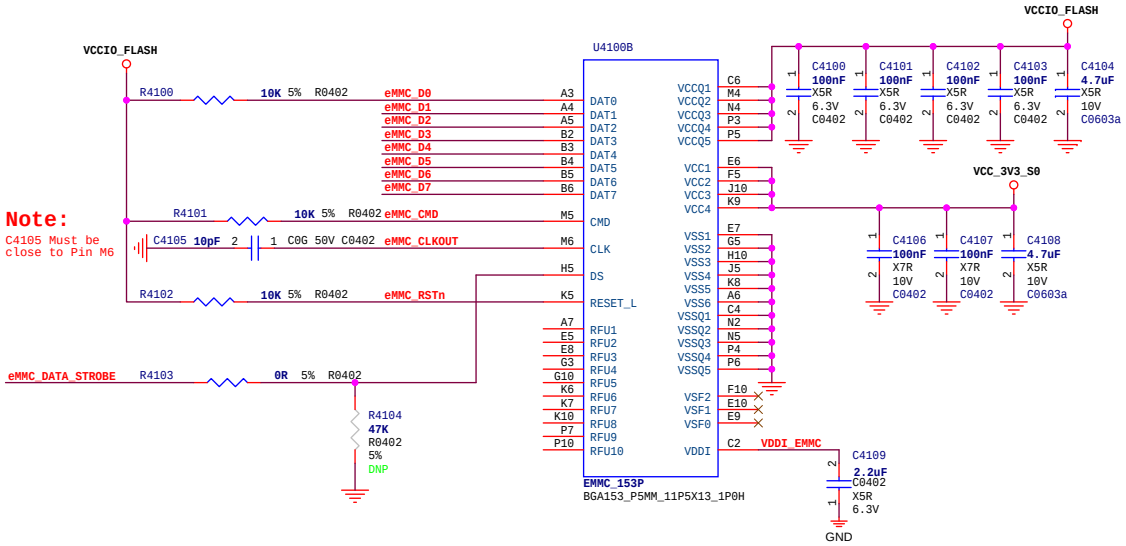
Flash Power

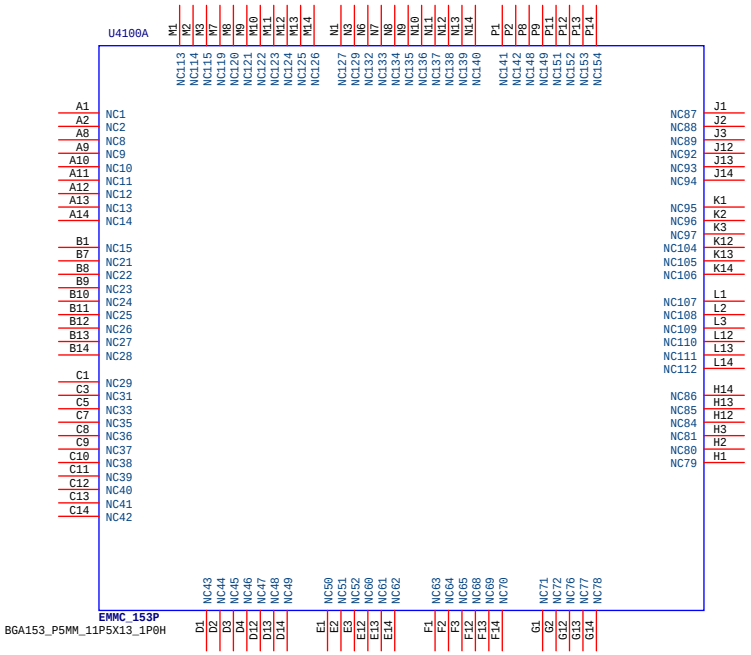


JWIPC Technology Co.,Ltd.		
Page Name: 27.Flash Power		
Size: A4	Project Name: 12C_RK3588S	Rev: V1.0
Date: Monday, June 27, 2022	Sheet 27 of 36	

eMMC Flash

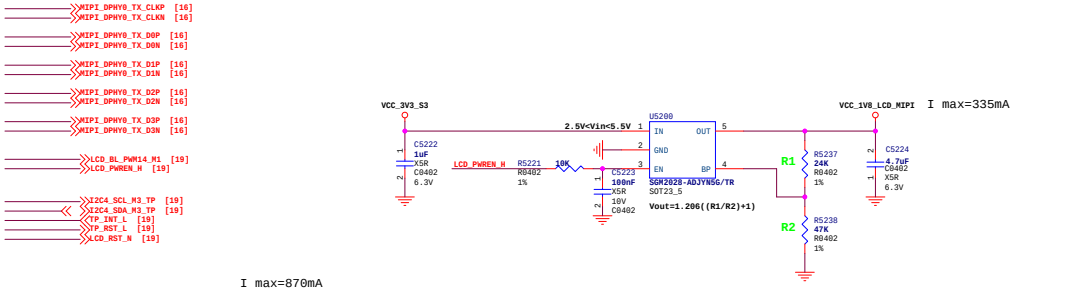




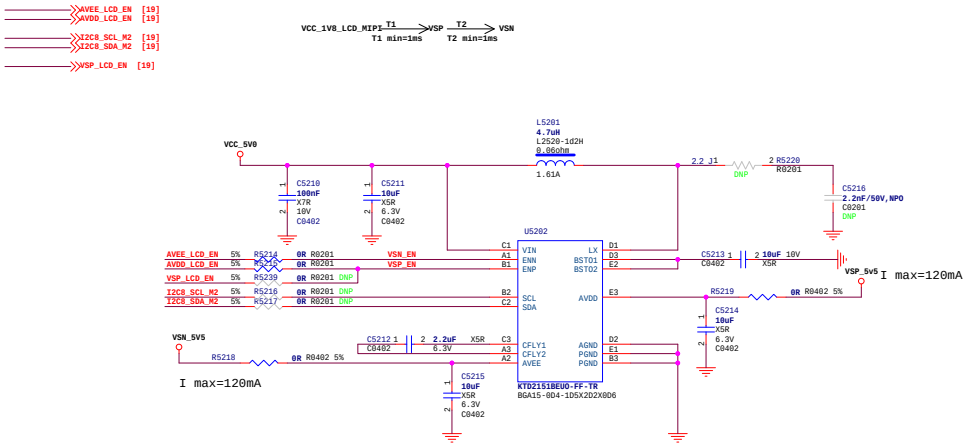


JWIPC Technology Co.,Ltd.		
Page Name: 28.eMMC Flash		
Size: A3	Project Name: 12C_RK3588S	Rev: V1.0
Date: Monday, June 27, 2022	Sheet 28 of 36	

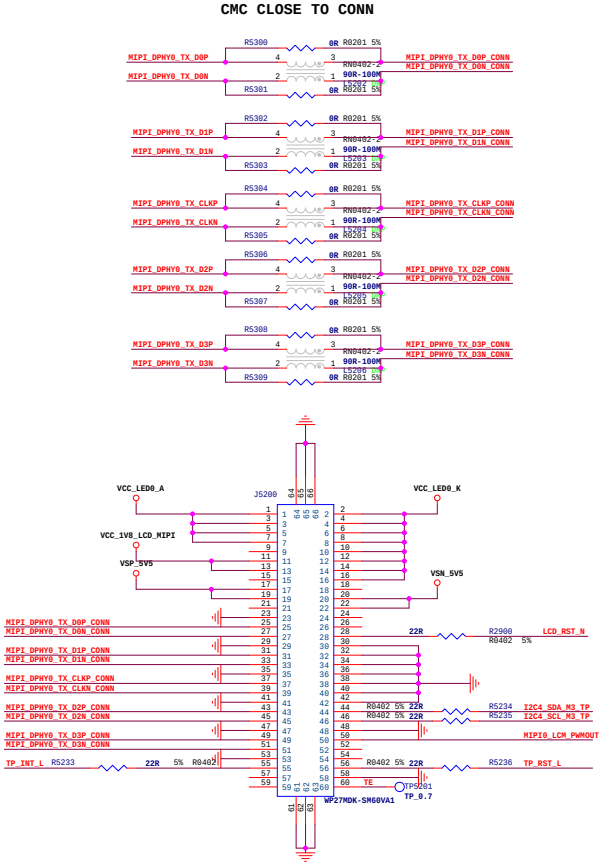
Single-MIPI LCM(MIPI DPHY0 TX)



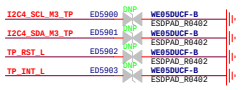
Positive / negative driven



LCM CONN



ESD



JWIPC Technology Co.,Ltd.			
Page Name	29.V0-LCM_MIPI_D/CPHY0_TX		
Size A2	Project Name 12C_RK3588S		Rev V1.0
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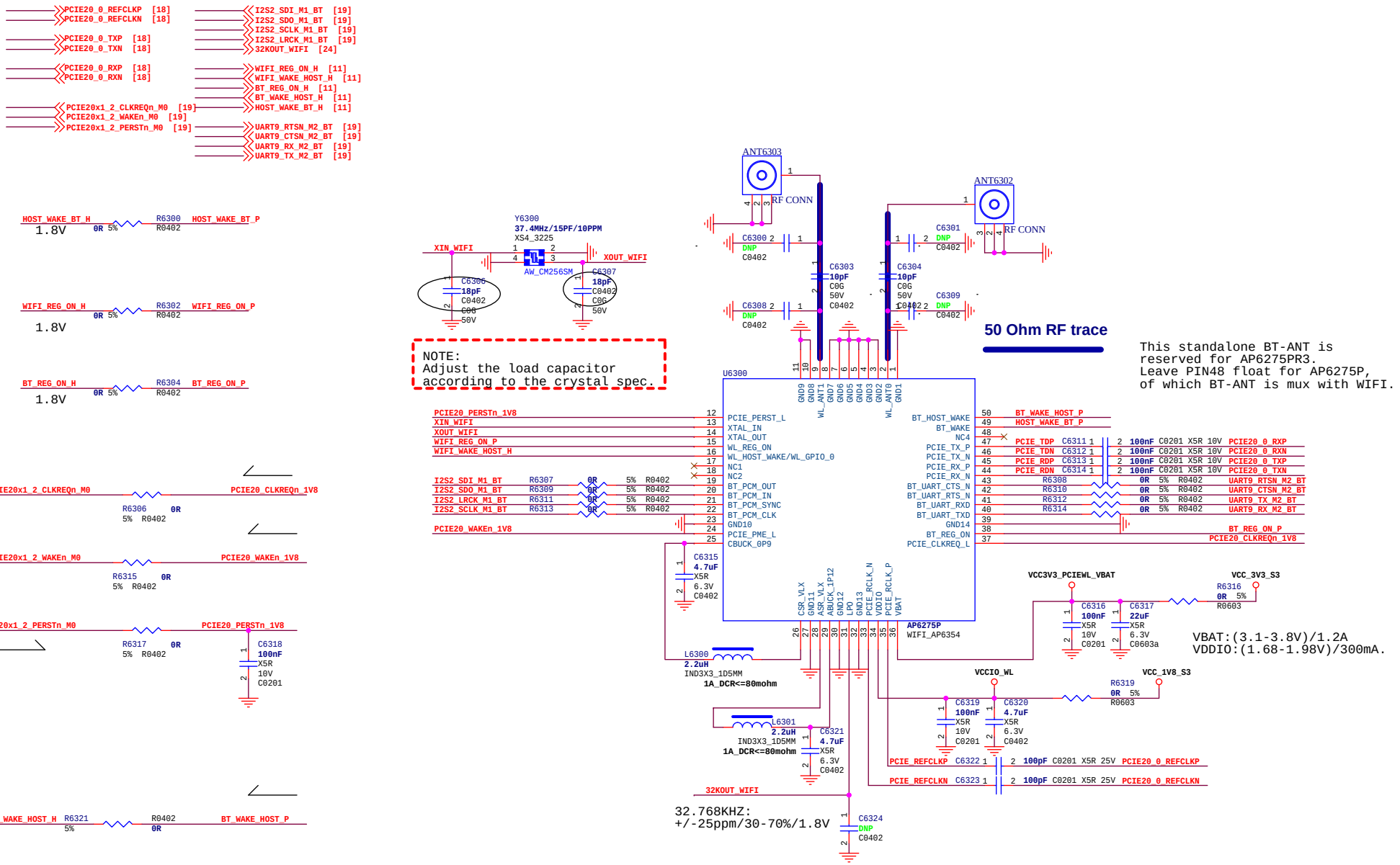
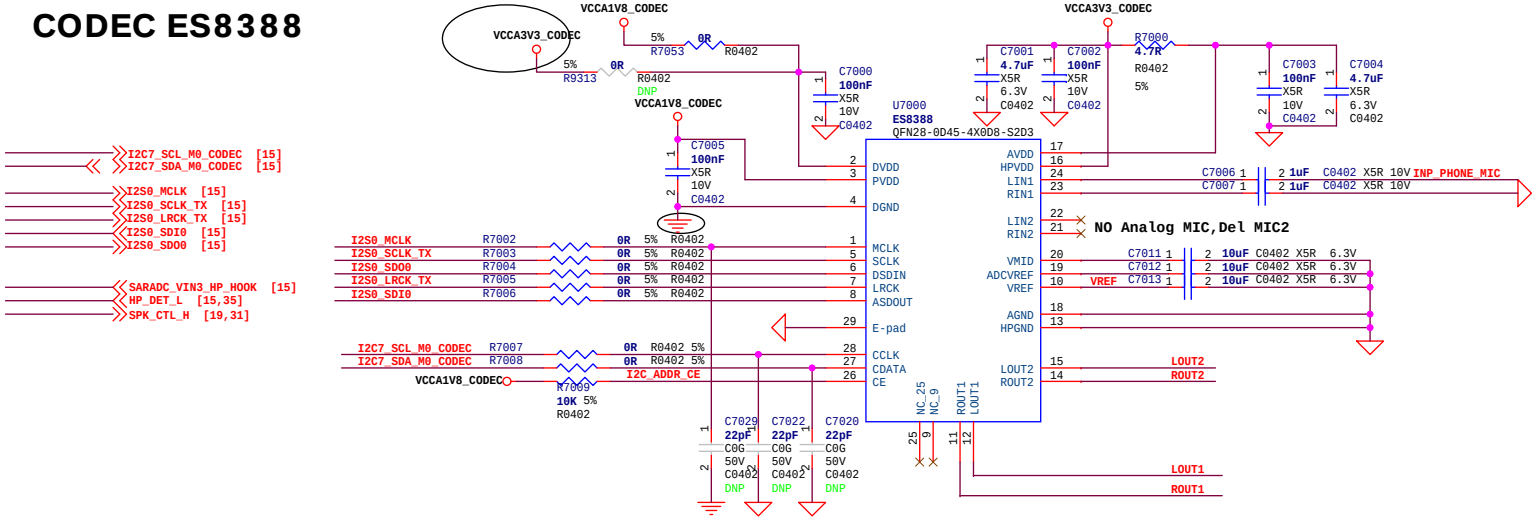
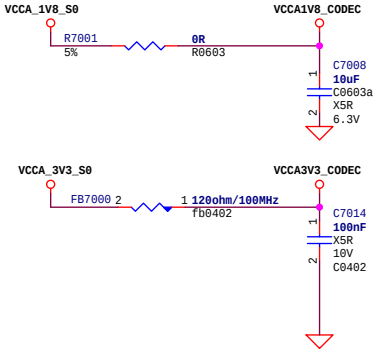
PCIe WIFI6/BT Module-2T2R



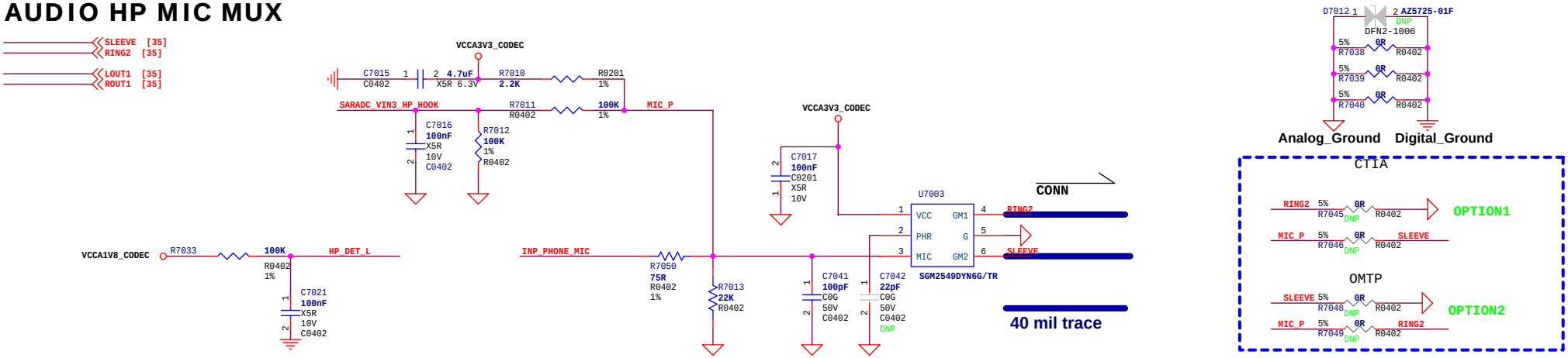
JWIPC Technology Co.,Ltd.		
Page Name: 30.WIFI/BT-PCIe_2T2R(opt2)		
Size: A3	Project Name: 12C_RK3588S	Rev: V1.0
Date: Monday, June 27, 2022	Sheet 30 of 36	

CODEC ES8388

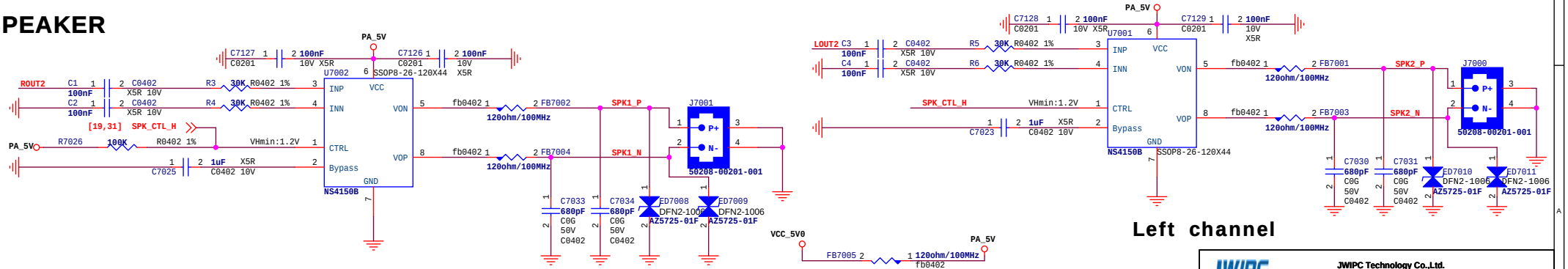




AUDIO HP MIC MUX



SPEAKER



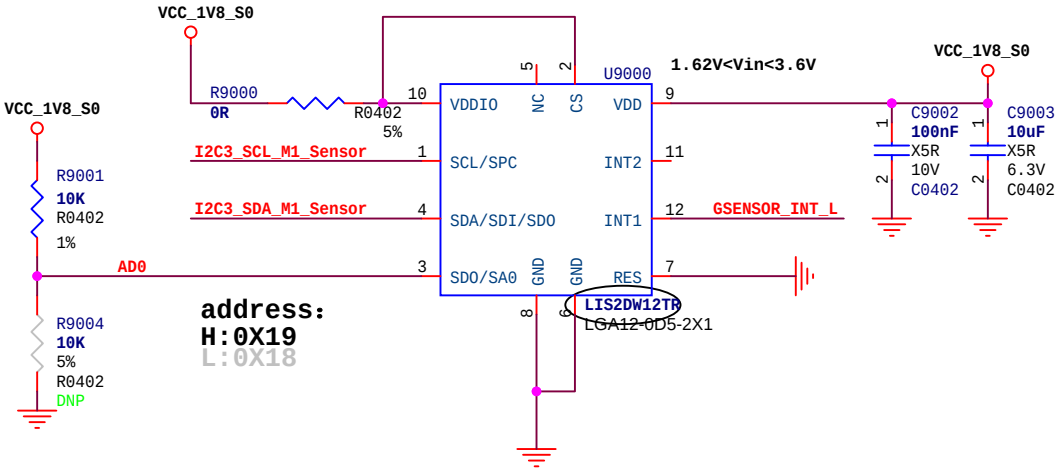
Right channel

Left channel

JWIPC	JWIPC Technology Co.,Ltd.	
Page Name	31.Audio Codec	
Size A3	Project Name 12C_RK3588S	Rev V1.0
Date: Monday, June 27, 2022	Sheet 31 of 36	

Gyroscope+G-sensor

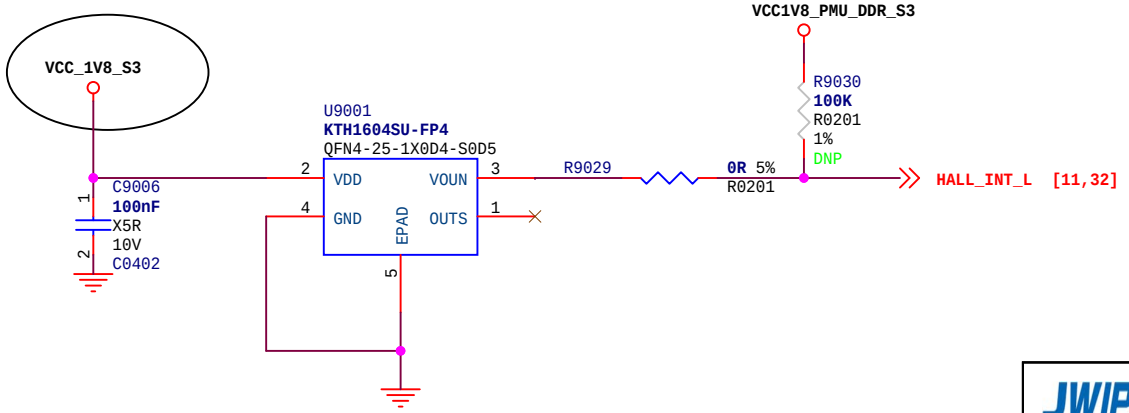
I2C3_SCL_M1_Sensor [19]
I2C3_SDA_M1_Sensor [19]
GSENSOR_INT_L [15]



Ambient Light+Proximity Sensor

HALL SENSOR

HALL_INT_L [11,32]



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32.Sensor

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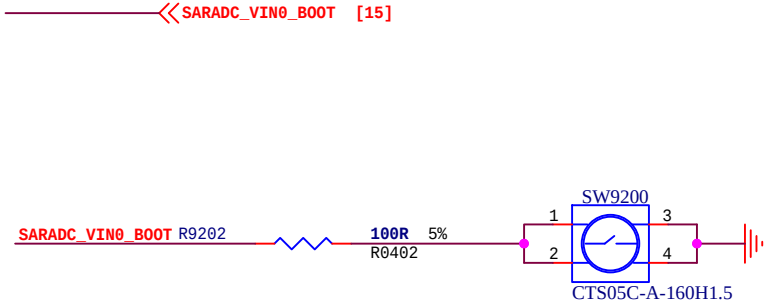
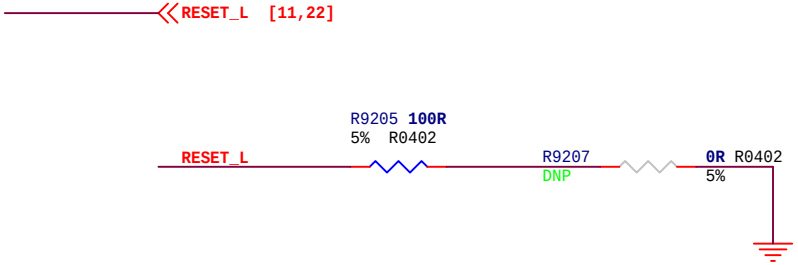
KEY Array move to DB

Maskrom Key



Note:
If BOOT_SARADC_IN0=0V after power-on reset, then system will enter into Maskrom mode.

Reset_Key



PWR_Key move to DB

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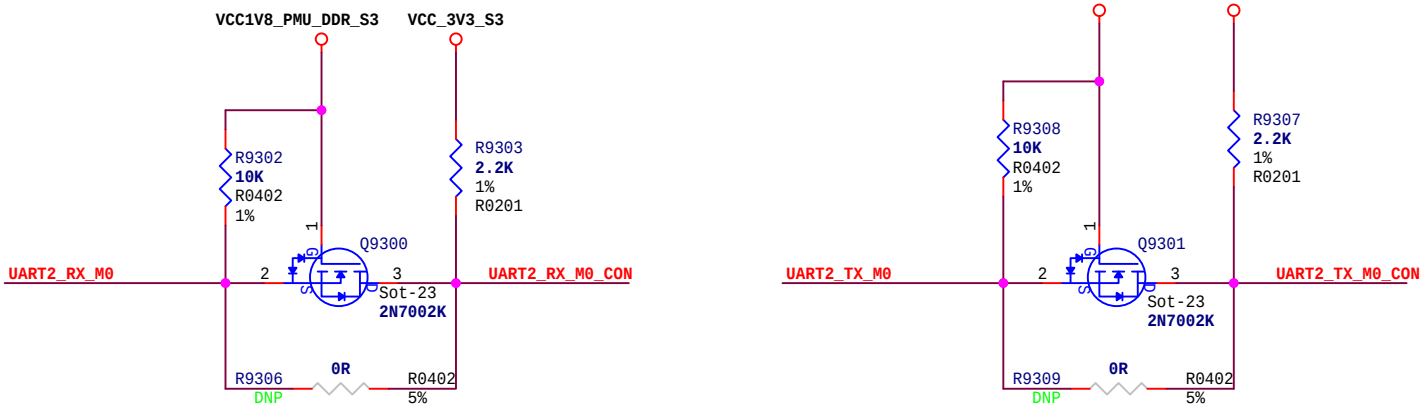
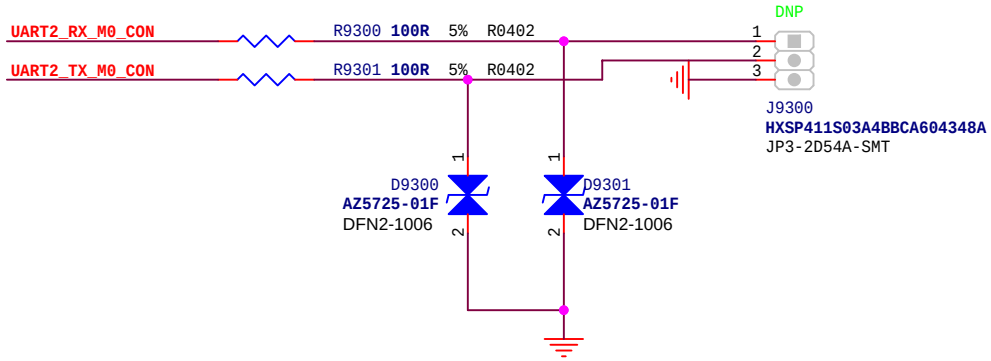
UART Debug

[11] UART2_TX_M0
[11] UART2_RX_M0





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34.UART Debug

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IO board conn

TYPEC_CC2_PORT [21]
TYPEC_CC1_PORT [21]
TYPEC0_SSTX1N [14]
TYPEC0_SSTX1P [14]
TYPEC0_SSRX1N [14]
TYPEC0_SSRX1P [14]
TYPEC0_SSTX2N [14]
TYPEC0_SSTX2P [14]
TYPEC0_SSRX2N [14]
TYPEC0_SSRX2P [14]
TYPEC_SBU1_PORT [21]
TYPEC_SBU2_PORT [21]
I2C6_SDA_M3 [19,21,24]
I2C6_SCL_M3 [19,21,24]
TYPEC0_OTG_DP [14]
TYPEC0_OTG_DM [14]

SIM_DATA [25]
SIM_CLK [25]
SIM_RST [25]
SDMMC_D0 [13]
SDMMC_D1 [13]
SDMMC_D2 [13]
SDMMC_D3 [13]
SDMMC_CMD [13]
SDMMC_CLK [13]
SDMMC_PWREN [19]
R_LED_L [19]
G_LED_L [19]
SLEEVE [31]
RING2 [31]
HP_DET_L [15,31]
LOUT1 [31]
ROUT1 [31]
PHONE_CTL [19]

Type C CONN

VBUS_TYPEC_P
VCC_3V3_S3
J9400
51540-03601-001
CNS36-0D5-UPF-51540

SIM&SD CARD_HP JACK CONN

USIM_VDD
VCC_3V3_S3
J9401
51540-03001-001
CNS30-0D5-UPF-51540

Sidekey conn

FP_1D8V_PWREN_H [19]
FP_2D8V_PWREN_H [19]
FP_SPI_MISO [19]
FP_SPI_MOSI [19]
FP_SPI_CLK [19]
FP_SPI_CS [19]
FP_EINT [19]
FP_RST_N [19]
SIM_DET_H [25]
SDMMC_DET_H [11]
SLP_S3_L [19]
PWRON_L [22]
SARADC_VIN1_KEY/RECOVERY [15]

Fingerprint/KEY CONN

VCC_5V0
J9402
51530-01401-001
CNS14-0D5-UPF-51530

SIM_DET_H R3501 0R R0201 5% SIM_SD_DET
SDMMC_DET_H R3502 0R R0201 5%
D3500 LRB521BS-30T5G sod882
SLP_S3_L PWRON_L

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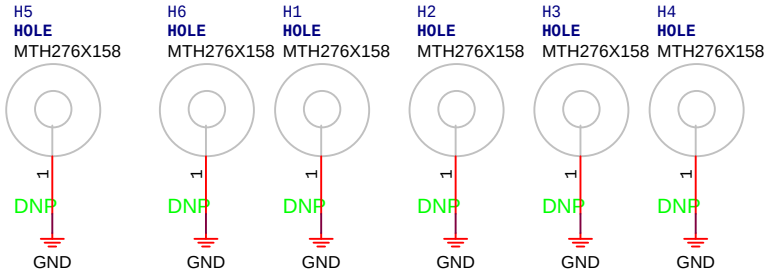
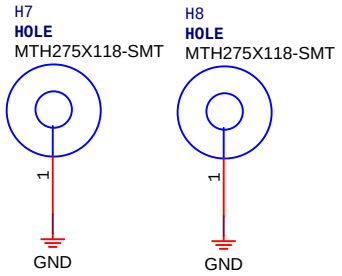
PCB Mark Point

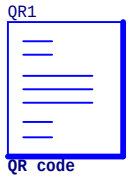
Mechanical Hole



Boss Crew



Shield



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